Design of Conditional Data Mapping Flip-Flop for Low Power Applications

Kanika Jindal, Renu, V. K. Pandey

Abstract*—Power consumption is a major bottleneck of system performance and it is listed as one of the top three challenges in International Technology Roadmap for Semiconductor 2008. In practice, a large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. In this paper, various design techniques for a low power clocking system are surveyed. Among them minimizing a number of clocked transistor is an effective way to reduce capacity of the clock load. To approach this, we propose a conditional data mapping technique which reduces the number of local clocked transistors. A 24% reduction of clock driving power is achieved.

Keywords: Flip Flop, Low Power, CMOS Circuit.

I. INTRODUCTION

THE SYSTEM-ON-CHIP (SoC) design is integrating hundreds of millions of transistors on one chip, while packaging and cooling only have a limited ability to remove the excess heat. All of these results in power consumption being the major bottleneck in achieving high performance and it is listed as one of the top three challenges in ITRS 2008. The clock system, which consists of the clock distribution network and sequential elements (flip-flops and latches), is one of the most power consuming components in a VLSI system [1], [2]. It accounts for 30% to 60% of the total power dissipation in a system [1]. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. A large portion of the on chip power is consumed by the clock drivers. Caution must be paid to reduce clock load when designing a clocking system. There is a wide selection of flip-flops in the literature [1]–[18]. Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops [2]. Traditional master-slave single-edge flip-flops, for example, transmission gated flip-flop [3], are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF) [4]. All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking [5]. Pulse triggered flip-flops could be classified into two types, implicit-pulsed and explicit-pulsed, for example, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) [6] and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO) [6].

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This paper surveys various low power techniques for the clocking system in Section II. After that we elaborate on the reduction of clock capacity to achieve low power in Section III. Section IV presents simulation results. Section V concludes this paper.

II. SURVEY OF LOW POWER DESIGN OF A CLOCKING SYSTEM

Power consumption is determined by several factors including frequency f, supply voltage V , data activity α, capacitance C, leakage, and short circuit current

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

In the above equation, dynamic power $P_{dynamic}$ is also called the switching power,

$$P_{dynamic} = \alpha CV^2 f.$$

$P_{short\ circuit}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while $P_{short\ circuit} = I_{short\ circuit} Vdd$.

$P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current. Sub threshold leakage is the dominant leakage now.

$$P_{leakage} = I_{leakage} Vdd.$$

Based on these factors, there are various ways to lower the power consumption shown as follows.

1) Double Edge Triggering: Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. For example, the clock branch shared implicit pulsed flip-flop [7] (CBS-ip DEFF), is a double edge triggered flip-flop. Double clock edge triggering method reduces the power by decreasing frequency f in equation.

2) Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip-flop. For example, low swing double-edge flip-flop (LSDFF) [8] is a low swing flip-flop.In addition, the level converter flip-flop is a natural candidate to be used in low swing environment too. For example, CD-LCFF-ip [9], could be used as a low swing flip-flop since incoming signals only drive nMOS transistors. The low swing method reduces the power consumption by decreasing voltage in equation.

3) There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional discharge flip-flop (CDFF) [10], conditional capture flip-flop (CCFF) [11]) or clock gating.

a) Conditional Operation.
For dynamic flip-flops, like hybrid latch flip-flop (HLFF) [12], semidynamic flip-flop (SDFF) [13], there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to control the redundant switching. For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when Q keeps 1. Internal node will not be kept discharging at every clock cycle. In CCFF, it uses a clocked NOR gate to control an nMOS transistor in discharging path when Q keeps 1. The redundant switching activity is removed in both cases. This reduces the power consumption by decreasing data activity in the equation.

b) Clock Gating.
When a certain block is idle, we can disable the clock signal to that block to save power. Gated master slave flip-flop was proposed in [14]. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

4) Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS technique [15] as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption [16]. A data retention flip-flop is proposed in [17].

5) Reducing Short Current Power: split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

6) Reducing Capacity of Clock Load: 80% of non clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity in equation. We will elaborate more in Section III.

III. REDUCING CLOCK CAPACITY BY MIMIMIZING THE NUMBER OF CLOCKED TRANSISTORS

A large part of the on-chip power is consumed by the clock drivers [18]. It is desirable to have less clocked load in the system. CDFF and CCFF in Section II both have many clocked transistors. For example,CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In contrast, conditional data mapping flip-flop (CDMFF, Fig.1) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF. (Note that CDFF used double edge clocking. For simplicity purposes, we did not include the power savings by double edge triggering on the clock distribution network). This shows the effectiveness of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDFF in view of power consumption [19], we do not discuss CCFF or CDFF further in this paper.

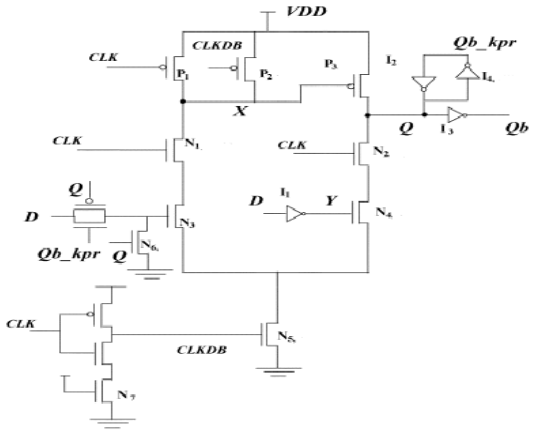

Fig1. CDMFF

However, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the precharging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here.

Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK transits from 0 to1, CLKDB will stay 1 for a short while which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND too. Hence internal node X is not connected with Vdd or GND during most pulse windows, it is essentially floating periodically. With feature size shrinking, dynamic node is more prone to noise interruption because of the undriven dynamic node. If a nearby noise discharges the node X, pMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nanoscale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point. For example, SDFF [13] has a keeper at node X while HLFF [12], and CCFF [11] have a transistor connecting to Vdd when D=0, respectively. Both methods serve to increase noise robustness of node X.

Finally it is difficult to apply the low power techniques introduced in previous section to CDMFF. For example, the clock structure with precharging transistors P1, P2 in CDMFF (Fig.2) makes it difficult to apply double edge triggering. Nor can CDMFF be used in a low swing clock environment.

(Note that the incoming low swing clock signal cannot drive pMOS, P1 and P2, in high voltage block (VDDH), because the pMOS transistors will not turn off by a low swing voltage, resulting in short circuit power consumption.)

IV. SIMULATION RESULTS

The simulation results for the flip-flop were obtained in a 0.18µm CMOS technology at room temperature using PSPICE, the supply voltage is 1.8 V.

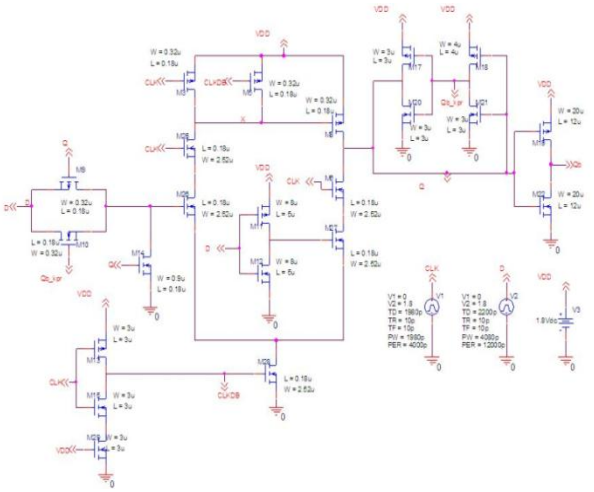

Fig2. PSPICE capture of CDMFF

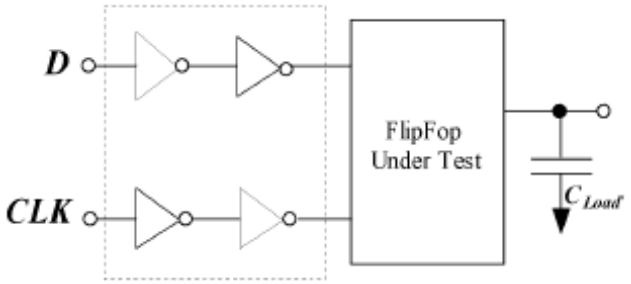

Fig3. Setup used for simulation

Fig4. Waveform for CDMFF

Fig5. Waveform for Power Consumption at process

V. CONCLUSION

We conclude this paper by outlining an important set of guidelines which are the corner stone for low power flip-flop design methodology and low power flip-flop simulation .In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits. Our experimental results enabled us to identify the power and performance trade-offs of the flip-flop design.

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