Comparative Study and Approach to Enhanced the Range and Power Requirement for Basic Memory Segment Analog Design

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Abstract—Now a day, analogy designing with dynamic range in high in demand. The minimum dissipation for power factor can be achieved only with improved range of system. Current mirror component is being researched from mainly of the years to achieve it’s grated extend voltage level for power consumption. To comparative study of various current mirror with enhanced technology top design analogy circuit of most extend. This paper comes with achieve a logic for the communication system to achieve such a system which can be run over low power and low voltage supply. This paper also includes the theorem and result table by which it is easy to access the need of such a technology. CMOS S-RAM design is the basic element of memory design which can be achieved and comparative study is also given to minimize future works.

Index Terms—VMS , Low Voltage Low Power Current Mirror , Basic Current Mirror

I. INTRODUCTION

The current mirror is one of most common building blocks both in analog and mixed mode VLSI circuits. Current mirror is a core structure for almost all analog and mixed circuits[1-4]. It determines the performance of analog structures, which largely depends on their characteristics [5, 6]. The design philosophy of analog circuits is now moving towards implementing them in the form of standard building blocks, called analog signal processing (ASP) cell rather than the desecrate circuits. The ASP cells, which consists of several basic analog circuit structures and have voltage mode or current mode circuits are described as the circuits whose input and output signal are in form of currents and their complete circuit function are described through the currents signal rather than the voltages signals. The analog signal processing deal with converting signals from one analog domain to another. The basic building blocks generally use more than one transistor and perform only one function. The current mirror is a current controlled current source. The motivation behind a current mirror is to sense the current from a “reference current source “and duplicate this reference current source to other locations, or generate an output current equal to input current multiplied by desired current gain factor, current mirror is also called current copier.

II. APPLICATION OF CURRENT MIRROR

Current mirror is an essential structure in most of the analog circuit applications, where the gain of the MOS can be expressed as product of its effective transconductance (g_m) and the output impedance (r_o). Due to continuous downscaling of MOS technology the device size is shrinking fast to enable higher unity gain frequencies. However, it reduces the gain of the MOS due to lowering of transconductance (g_m) and increase in output conductance (1/r_o) [1 & 2]. The speed and accuracy of analog circuit structures are determined by its settling behavior. Fast settling demands high unity gain frequency and a single pole frequency response, whereas accurate settling requires high d.c. gain. In Figure 2 the block diagram of the application of current mirrors in analog circuits is shown. Current mirrors are essential blocks of analog circuits and mixed circuit like op amp, oscillator, and regulator. Some of important applications are discussed below:
III. HIGH SPEED AND LOW POWER

As the feature size of CMOS which processes reduces, which includes supply voltage has to be reduced for the reduction of power dissipation by per unit cell. Which results from device scaling. However, the circuit’s performance goes down by degrading this current mirror. The reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces minimum risk to the thinner oxides. By scaling down the threshold voltage of the MOSFETs reduces the performance loss (degraded bandwidth, low voltage swing etc.) somewhat but it has its own disadvantages i.e. the increase in the static power dissipation. On other hand, The non-zero current of MOSFETs in OFF state in digital circuits

- A Short-circuit power consumption due to the current flowing during the lapse of time when both NMOS and PMOS transistors are in the on state.

The dynamic power expenditure has been increasing quickly along with the progress in the processing technology of CMOS, which raises the ambient temperature and minimize the device performance and the circuit performance is less stable. By reducing power supply voltage is the most efficient method in reducing power dissipation of a chip. The dynamic power dissipation is given by

\[ P = \alpha C_L V_{DD}^2 f_{CLK} \]

where \( \alpha \) is the probability of the logic gate output to change from 0 to 1 and hence its value ranges from 0 to 1 and is called the switching activity, \( C_L \) is the load capacitance, and \( f_{CLK} \) is the clock frequency. Due to enhanced demands on the system performance, the clock frequency increases. By which Power dissipation can be reduced by reducing the switching activity and the output load capacitance. The previous can be reduced via proper circuit and system designs and the latter can be by reducing device dimensions or reduced by an advanced CMOS technology. But the reduction in power dissipation is most effective when \( V_{DD} \) is lowered. The static power consumption depends on the OFF state current (I_{on}) and equals

\[ P_{static} = I_{on} V_{DD} \]

For conventional CMOS technologies with high threshold voltages, this contribution is too low. In case of analog circuits it is the main contributor for power dissipation as the devices are biased permanently in saturation modes. During switching in CMOS, both PMOS and NMOS are simultaneously active for a short period of time and an instantaneous short-circuit current (I_{sc}) flows from the power supply directly to ground. So the power consumption due to I_{sc} is given by

\[ P_{sc} = I_{sc} V_{DD} \]

This term can be neglected if the signals have short rise and fall times as compared to duration of the signal. Thus, the total power consumption is as given

\[ P_{total} \approx N_{eq} V^2 + I_{off} V_{DD} \]
The operation is not directly depend on the power supply. The analog circuits should have output voltage swing capability for high SNR (signal to noise ratio) and rail-to-rail input, which can be received using the CMCs. CMC structure is current conveyor (CC) \[11\].

- Very high output impedance (high \(R_{\text{out}}\) and low \(C_{\text{out}}\)). As a result the output current is independent of output voltages.
- Low input resistance (\(R_{\text{in}}\)).
- Low output and input compliance voltages.

I. LOW VOLTAGE CURRENT MIRROR DESIGNING TECHNOLOGY

At low voltage, the main constraints faced are the device noise level and the threshold voltage (\(V_T\)). Reduction in \(V_T\) is dependent on the technology of the device. On other hand Higher \(V_T\) gives better noise immunity and the lower \(V_T\) reduces the noise margin to result in poor SNR. Hence, for present day CMOS technology, reduction in \(V_T\) is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits. The restriction on further reduction in \(V_T\) paves the way to have simpler, smarter and efficient circuits complex circuits. The restriction on further reduction in \(V_T\) paves the way to have simpler, smarter and efficient circuits.

The low voltage cascode current mirror shown in figure 3. We assumes that the current mirror transistors M1 and M2 have identical, aspect ratio \(A_M = \frac{W_1}{L_1} = \frac{W_2}{L_2}\) Where \(W_1\) and \(W_2\) are the transistor channel width and \(L_1\) and \(L_2\) are the transistor length. Similarly the transistor M3 and M4 are assumed the same aspect ratio \(A_C = \frac{W_3}{L_3} = \frac{W_4}{L_4}\). The aspect ratio \(A_M\) may be different from the aspect ratio \(A_C\). In the analysis of the dynamic range the same aspect ratio of \(A_M\) and \(A_C\) and we use standard Schman –Hodges transistor model for the transistor in the saturation region and we neglected the bulk effect and assume that all the NMOS transistors have the identical.

Low voltage current mirror input current \(I_{\text{in}}\) we find the gatesource voltages and drain -source voltages

\[
V_{GS1} = V_{TS} + \frac{2I_{\text{in}}}{\sqrt{K_{AM}}} \quad (5)
\]

G to S voltage of transistor multiplier 3

\[
V_{GS3} = V_{TS} + \frac{2I_{\text{in}}}{\sqrt{K_{AC}}} \quad (6)
\]

D to S voltage of transistor multiplier 1 is

\[
V_{DS1} = V_{BS} - V_{TS} - \frac{2I_{\text{in}}}{\sqrt{K_{AC}}} \quad (7)
\]

Drain to source voltage of transistor multiplier 3 is

\[
V_{DS3} = V_{GS3} - V_{DS1} = 2V_{TS} - V_{BS} + \frac{2I_{\text{in}}}{\sqrt{K}} \frac{1}{\sqrt{K_{AM}}} + \frac{1}{\sqrt{K_{AC}}} \quad (8)
\]

Where, \(V_{TS}\) is the transistor threshold voltage, \(V_{BS}\) is the bias or gate voltage of transistor M3 and M4 and K is the transconductance parameter. Requiring \(V_{DS} - V_{TS} \leq V_{DS}\) for both M1 and M3 result in:

\[
\frac{2I_{\text{in}}}{\sqrt{K}} \left( \frac{1}{\sqrt{K_{AM}}} + \frac{1}{\sqrt{K_{AC}}} \right) + V_{TS} \leq V_{BS} \quad (9)
\]

Biasing voltage:

\[
V_{BS} \leq 2V_{TS} + \frac{2I_{\text{in}}}{\sqrt{K_{AM}}} \quad (10)
\]

In figure 3 low voltage current mirror, biasing voltage \(V_B\) is fixed when \(I_{\text{in}}\) increases, voltage of the gate –source voltage \(V_{GS3}\) of transistor M3

![Figure 3: Low Voltage Current Mirror](image-url)}
and $V_{in}$ will increase, and voltage level at the drain terminal of M1 decreases. Therefore M1 enter the triode region which determine upper limit of $I_{in}$. Below equation (11) ensure the saturation of M1 and determines the maximum value of $I_{in}$ for given value of the cascode bias voltage $V_{b}$ we have

$$I_{in,max} = \frac{K}{2} A_M \left( V_B - V_{th} \right)^2 \left( \frac{\sqrt{A_C/A_M}}{1 + \sqrt{A_C/A_M}} \right)^2$$  \hspace{1cm} (11)

Equations (9) ensure the saturation of M3 and determine the minimum value of $I_{in}$. We find

$$I_{in,min} = \frac{K}{2} \left( V_B - 2V_{th} \right)^2 A_M$$  \hspace{1cm} (12)

Maximum value of the bias voltage even at the minimum value of input current equation (10) determine, and equation (10) determined the value of $A_C$ and $A_M$ which determined the saturation of M1 and the maximum value of input current. To ensure Saturation operation of transistors M1 and M3 the input current range determined by

$$\frac{K}{2} \left( A_B - 2V_{th} \right)^2 \leq I_{in} \leq \frac{K}{2} A_M \left( V_B - V_{th} \right)^2 \left( \frac{\sqrt{A_C/A_M}}{1 + \sqrt{A_C/A_M}} \right)^2$$  \hspace{1cm} (13)

In a practical design procedure equation(10) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3 even at the minimum value of input current, and equation (11) can then be used to determine values of $A_C$ and $A_M$ which will ensure saturation of M1, even at the maximum value of input current.

In the important special case of $I_{in,min} = 0$ we find from (12) $V_B \leq 2V_{th}$. From equation (11) we then find the following design constraint on $A_C$ and $A_M$

$$A_M \left( \frac{\sqrt{A_C/A_M}}{1 + \sqrt{A_C/A_M}} \right)^2 \geq \frac{2I_{in,max}}{V_{th}}$$  \hspace{1cm} (14)

Assuming as a typical case $W_1 = W_3$ and $L_1 = L_3$ i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = A = \frac{V}{2} \geq \frac{2I_{in,max}}{V_{th}}$$  \hspace{1cm} (15)

For such case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{GS1} - V_{th} = \frac{2I_{in}}{\sqrt{A}} \geq \frac{V_{in}}{\sqrt{A_{in,max}}}$$  \hspace{1cm} (16)

So, case the minimum output voltage of the current mirror is and is independent of the input current.

$$V_{out,min} = V_B - V_{th} = V_{in}$$  \hspace{1cm} (17)

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage mismatch. It is evident that the effective gate-source voltage $V_{GS1} - V_{th}$ can be increased above the value given by equation(17) if $A_C$ is increased, i.e. a larger aspect ratio is used for the cascode transistor. In this case the cascode transistor requires a smaller effective gate-source voltage for a given value of input current, leaving more headroom for the drain-source voltage of the mirror transistor. Introducing $N = A_C/A_M$ we find

$$A_N = \left( \frac{1+V}{V} \right)^2 \frac{2I_{in,max}}{\left( V_B - V_{th} \right)^2}$$  \hspace{1cm} (18)

And

$$V_{GS1} - V_{th} = \frac{N}{1+N} \left( V_B - V_{th} \right) \frac{I_{in}}{V_{in,max}}$$  \hspace{1cm} (19)

Very low power signal output resistance of the mirror is given by

$$r_{out} = \frac{1}{\sqrt{g_{ds} g_{ds}} \left( \frac{1+V}{V} \right)^2} \frac{1}{g_{ds}} \frac{1}{g_{ds}}$$  \hspace{1cm} (20)

As $g_{ds}/g_{ds}$ is inversely proportional to the square root of $N$, we find that the output resistance is inversely proportional to $N$. Thus, the higher effective gate-source voltage of the mirror transistors is achieved at the expense of a reduced output resistance.

### III. DYNAMIC RANGE CALCULATION OF LOW VOLTAGE CURRENT MIRROR

Aspect ratio of transistors used in low voltage current mirror is given in table 2

<table>
<thead>
<tr>
<th>MOSFETs</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>NMOS</td>
<td>20µm</td>
<td>0.5µm</td>
</tr>
<tr>
<td>M5</td>
<td>PMOS</td>
<td>10µm</td>
<td>0.3µm</td>
</tr>
</tbody>
</table>

Table 2: Aspect Ratio in LVCM current mirror

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.0 volt</td>
</tr>
<tr>
<td>$V_{bias}$ (Voltage bias)</td>
<td>-0.2 volt</td>
</tr>
<tr>
<td>Threshold voltage $V_{in}$ (NMOS)</td>
<td>0.44 Volt</td>
</tr>
<tr>
<td>Transconductance</td>
<td>156.8µA</td>
</tr>
</tbody>
</table>

Table 3: Parameters used in Low Voltage Current Mirror (LVCM)

### IV. CONCLUSION

CMOS technology had already dominated the whole electronic industry. Demands on portable electronic devices, leads VLSI design to reducing power and increasing speed of electronic devices. With the advent of the portable electronic and mobile communication systems low-voltage and low-power mixed mode circuit design has gained importance. For the operation of such systems like hearing aids, implantable cardiac pacemakers, cell-phones and hand held multimedia terminals etc. battery is the main source of power. They require low power dissipation so as to have reasonable battery life and weight. Designing High Performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in analog circuit design is the current mirror. The current mirror is one of most common building blocks both in analog and mixed mode VLSI circuits. The applications of battery powered analog and mixed mode electronic devices require designing current mirror circuits to operate at low voltage levels.

### REFERENCES


AUTHOR PROFILE

Mr. Naveen Kumar is a student of final year Master of Technology at Applied College of Management and Engineering. His area of interest is Memory Application and Low Voltage Device.