Simulation Study of a Monopole HVDC Transmission System Feeding a Very Weak AC Network with Firefly Algorithm Based Optimal PI Controller

S. Singaravelu, S. Seenivasan

Abstract*— This paper presents a simulation study of a line commutated converter (LCC) –monopole HVDC transmission system feeding a very weak AC network with firefly algorithm based optimal proportional integral (PI) controller for the rectifier and the inverter control and hybrid reactive power compensators (RPC's) at the inverter AC side. The hybrid compensator is an equal mix of fixed capacitor (FC) with any one of the following compensators: synchronous compensator (SC); static var compensator (SVC); static synchronous compensator (STATCOM). The HVDC transmission system model is simulated using Matlab. The transient performances of hybrid RPC's (FC+SC, FC+SVC and FC+STATCOM) are investigated during various fault conditions and the results are compared with the performance of the SC, SVC and STATCOM to focus the supremacy of the hybrid compensators. The simulation results confirm that the equal combination of FC and STATCOM has a steady and fastest response. The outcomes also demonstrate the superiority of the firefly algorithm based optimal PI controller over the conventional PI controller. The harmonic present in the inverter AC side is also observed under steady state operation to assure the quality of power supply.

***Index Terms*- Firefly algorithm, Hybrid RPC's, Monopole HVDC, PI controller, Very weak AC system.**

I. INTRODUCTION

Due to the rapid growths in the voltage, power carrying capacity and length of transmission lines, the HVDC power transmission technology is now emerging [1]. The behaviour of the HVDC system plays ever greater roles in the performance of entire AC/DC power systems. It is essential to understand the mechanisms of the interactions between an HVDC system and an AC network so the HVDC system can be operated in a manner that enriches the stability of the entire power grid. The significance of this interaction [2] largely depends on the strength of the AC system at the converter bus, which is presented by the short circuit ratio (SCR). The following SCR values [3] can be used to classify AC systems: a) SCR >3 for a strong system, b) 2 ≤ SCR < 3 for a weak system, c) SCR < 2 for a very weak system.

Several works have been accomplished to identify the interaction between AC networks and HVDC systems. The performance of the HVDC system under AC and DC disturbances [4] is analyzed with dynamic voltage control devices at the inverters of very weak AC systems by considering the compensators: Fixed capacitor (FC), SC, SVC and a mix of the SC and SVC. The feasibility to interconnect AC/DC systems, leading to very weak short circuit ratios (SCRs) lower than 1.5 [5] is exposed with STATCOM for reactive power compensation. A multilevel gate turn-off (GTO) thyristor inverter as an advanced static var compensator [6] is proposed for HVDC system and the suppression of temporary over voltage (TOV) and DC power recovery performance of the advanced static var compensator investigated at an HVDC converter terminal, with a very low SCR AC system and the simulation results are compared under various AC and DC disturbances with the reactive power compensation options available. To make the analysis complete, it is highly necessary to consider the suppression of TOV and fault recovery performances for an HVDC system feeding a very weak AC network with the following hybrid RPC's as well, FC+SC, FC+SVC and FC+STATCOM. Thus, in this simulation work transient performance has been carried out for an HVDC transmission system connected to very weak AC network with the following RPC's: SC, SVC, STATCOM, FC+SC, FC+SVC and FC+STATCOM. The harmonics investigation is also done under steady state to insure the quality of power supply on inverter AC side.

The conventional PI controller used for rectifier and inverter controllers of HVDC system causes instability due to deficiency in tuning its gain during abnormal conditions. To overcome this drawback intelligent technique [7-10], are introduced for proper tuning of the PI controller parameters. However, in all those tuning methods the principal signals used to fix the PI gains of the rectifier and the inverter current controllers are current error and its derivative. For the inverter gamma controller, the gamma error and its derivative are used. In this paper, minimization of the rectifier and the inverter DC power errors are considered as an objective function which is achieved by the firefly optimization algorithm, to fix the PI gains of the respective PI controller. To demonstrate the effectiveness of firefly algorithm based optimal PI controller, on transient performance, it has been compared with conventional PI controller.

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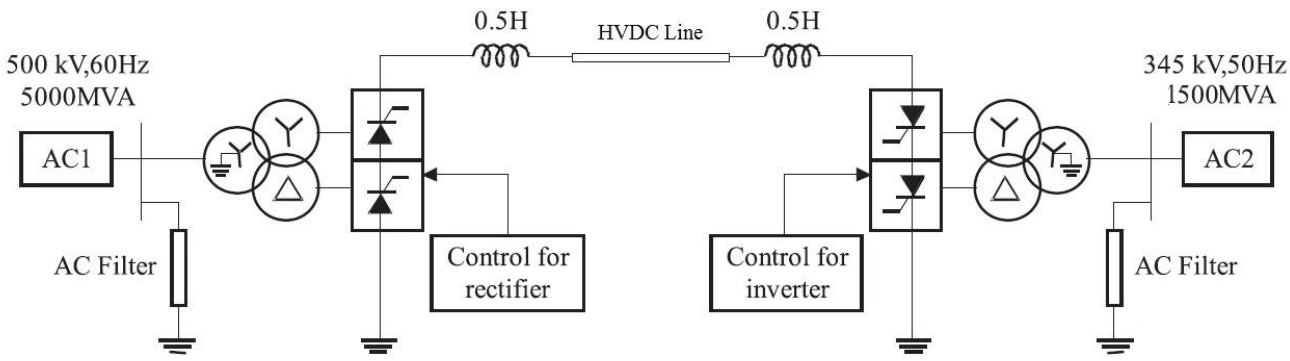

Fig. 1: Monopole HVDC transmission system model feeding a very weak AC network.

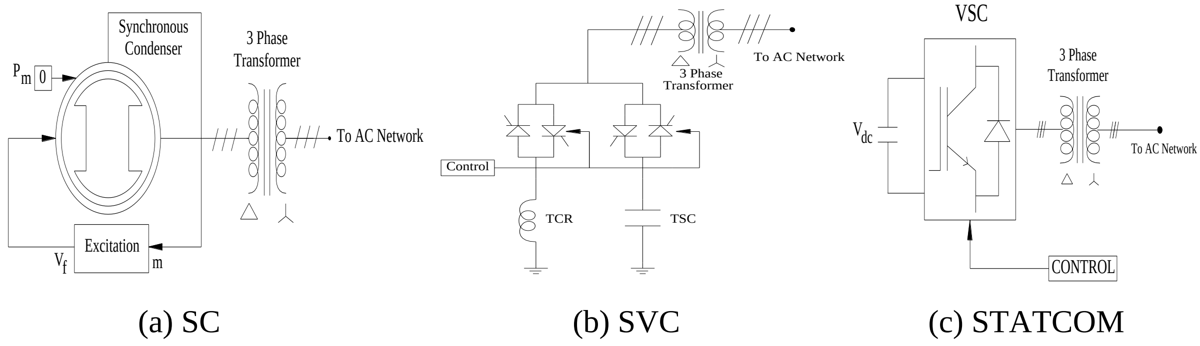

Fig. 2: Schematic of RPC‘s.

II. MODELLING OF MONOPOLE HVDC TRANSMISSION SYSTEM

A line commutated converter based monopole HVDC system of 500kV, 2kA, 1000MW feeding a strong AC network [11], in which inverter side AC network is replaced by a very weak AC network as shown in the Fig.1. The rectifier side AC system of 500kV, 5000MVA, 60Hz is connected to the inverter side AC system of 345kV, 1500MVA, 50Hz through an HVDC network. Generally, the AC system is represented by damped LLR equivalents. The Passive filters of 450MVAr are connected on the source side to eliminate the 11th and 13th (the double tuned type) order and above 24th (second order high pass filter) order current harmonics and synchronous or static compensator or fixed capacitor with synchronous or static compensator is used (150MVAr) for reactive power compensation. The rectifier and the inverter are 12-pulse converters.

The DC network model consists of a smoothing reactor for the rectifier and the inverter bridges, a passive filter of double tuned type to mitigate the 12th and 24th order DC voltage harmonics and the DC line. The DC link of 1500 km is modelled as a distributed parameter line model with lumped losses. The rectifier is equipped with a current controller to maintain the DC system current constant. The inverter is provided with a current controller to maintain the DC system current constant and a constant extinction angle or gamma controller. The reference current for the current controllers is obtained from the master controller output through the voltage dependent current order limiter (VDCOL). In order to protect the rectifier and the inverter DC protection functions are implemented in each converter.

In the inverter side AC network, the following six reactive power compensator options are studied.

A. Synchronous Compensator

The SC model of 150MVAr shown in Fig. 2 (a) is represented with the simplified synchronous machine block which models, both the electrical and mechanical characteristics of a simple synchronous machine. The SC uses the solid static excitation system.

B. Static Var Compensator

A 150MVAr SVC shown in Fig. 2 (b) regulates voltage on a 345kV system. The SVC consists of a 345kV/16kV, 168MVA coupling transformer, one 60MVAr TCR bank and one 180MVAr TSC connected to the secondary side of the transformer. Switching the TSC in and out allows a continuous variation of the secondary reactive power from zero to 180MVAr capacitive, whereas phase control of the TCR allows a continuous variation from zero to 60 MVAr inductive.

C. Static Synchronous Compensator

The STATCOM shown in Fig. 2 (c) is located at the inverter side of the HVDC link and has a rating of ±150MVAr. This STATCOM is a typical simple PWM voltage source converter (VSC). It consists of a 6 pulse VSC inverter and a series connected capacitors which act as a variable DC voltage source. Based on a VSC, the STATCOM regulates system voltage by absorbing or generating reactive power.

D. An Equal Mix of FC and SC

The FC (75MVAr) and SC (75MVAr) are connected to the inverter bus in this scheme. In steady state the FC and SC each supply 75MVAr.

E. An Equal Mix of FC and SVC

The FC (75MVAr) and SVC (-90MVAr, +30MVAr) are connected to the inverter bus in this scheme. In steady state the FC and SVC each supply 75MVAr.

F. An *Equal* Mix of FC and STATCOM

The FC (75MVAr) and STATCOM (±75MVAr) are connected to the inverter bus in this scheme. In steady state the FC and STATCOM each supply 75MVAr.

III. APPLICATION OF FIREFLY ALGORITHM FOR OBTAINING OPTIMAL GAIN VALUES FOR PI CONTROLLERS

In this paper, an optimization of the rectifier and the inverter side DC power error is picked as a prime objective function which has to be minimized. To achieve the same DC power (P_{DCMEA}) and its reference (P_{DCREF}) is compared to get the error signal. The integral square error of the rectifier DC power error and inverter DC power error are processed by the firefly algorithm [12-14], to fix the gain of the rectifier current PI controller and to fix the gain of the both inverter current PI controller and the gamma PI controller respectively. This approach ensures the reduced computational procedure, faster recovery and reduced TOV. The schematic diagram of the firefly algorithm based tuning technique is shown in Fig. 3. The general flow chart for minimization of the rectifier/ the inverter DC power error function using firefly algorithm is shown in Fig. 4.

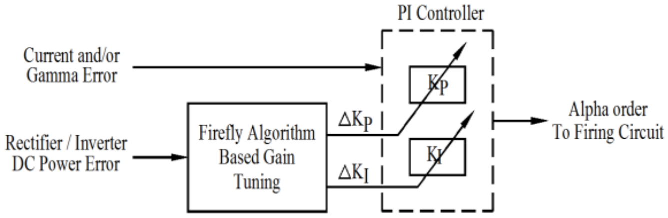

Fig. 3: Schematic Diagram of the Firefly Algorithm Based Tuning Technique

IV. SIMULATION RESULTS AND DISCUSSION

In order to know the interaction between AC network and HVDC systems, MATLAB simulation model is implemented based on the data [15]. At the inverter AC Side, SC, SVC, STATCOM, FC+SC, FC+SVC and FC+STATCOM are the various RPC's considered for analysis. In all the cases simulated steady state AC voltage and current waveforms at the inverter AC side and their harmonic spectrums are observed to assure the quality of the AC supply. The transient performance of the HVDC system is analyzed in the presence of various RPC'S for a duration of two seconds under different fault conditions to study the suppression of TOV and fault recovery. For the purposes of comparison, identical fault duration of 0.05seconds was used for all types of faults. The inverter side RMS AC voltage waveforms are observed during various AC faults and DC fault on the rectifier side to study the TOV suppression capability of the proposed firefly algorithm based PI controller. For analyzing the fault recovery capability with the proposed firefly algorithm based PI controller, the inverter DC power is observed, under various AC faults and DC faults at rectifier and inverter side. In all the cases, the TOV suppression and fault clearance capability of the firefly algorithm based PI controller are compared with conventional PI controller of an HVDC transmission system.

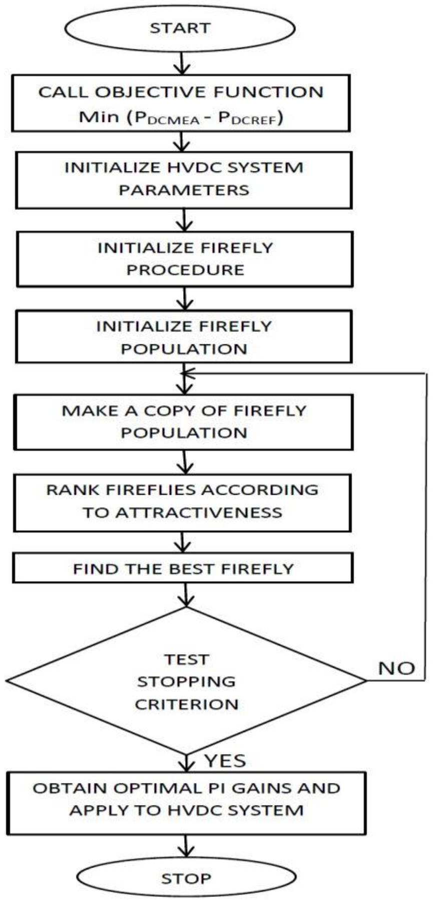

Fig. 4: Flowchart for minimization of the rectifier/the inverter DC power error function using firefly algorithm

A. Inverter Side AC Harmonics

The inverter side AC voltage and current waveforms and their harmonic spectrums during steady state operation are shown in Fig. 5, 6 and the results are listed in table I. From the inverter side AC waveforms and their harmonic spectrum, it is found that in all the cases the voltage and current are equal to 1p.u and the harmonics are within tolerable limit. The 11th and 13th current harmonics are the foremost harmonics on the inverter AC side.

B. Temporary overvoltage

When disturbances occur on the DC line or at the rectifier side, commonly temporary over voltage happens. It is usual practice a large number RLC based filters are provided in the inverter side of the HVDC system, in order to supply the part of necessary reactive power. During rectifier side AC or DC faults (the inverter side has no faults), the DC is blocked, and hence the reactive power of those filters will flow into the AC system, which often causes TOV. In order to suppress the TOV, the reactive power compensator and DC system PI controllers should respond quickly otherwise the TOV could be very high and could damage the insulation of the equipment.

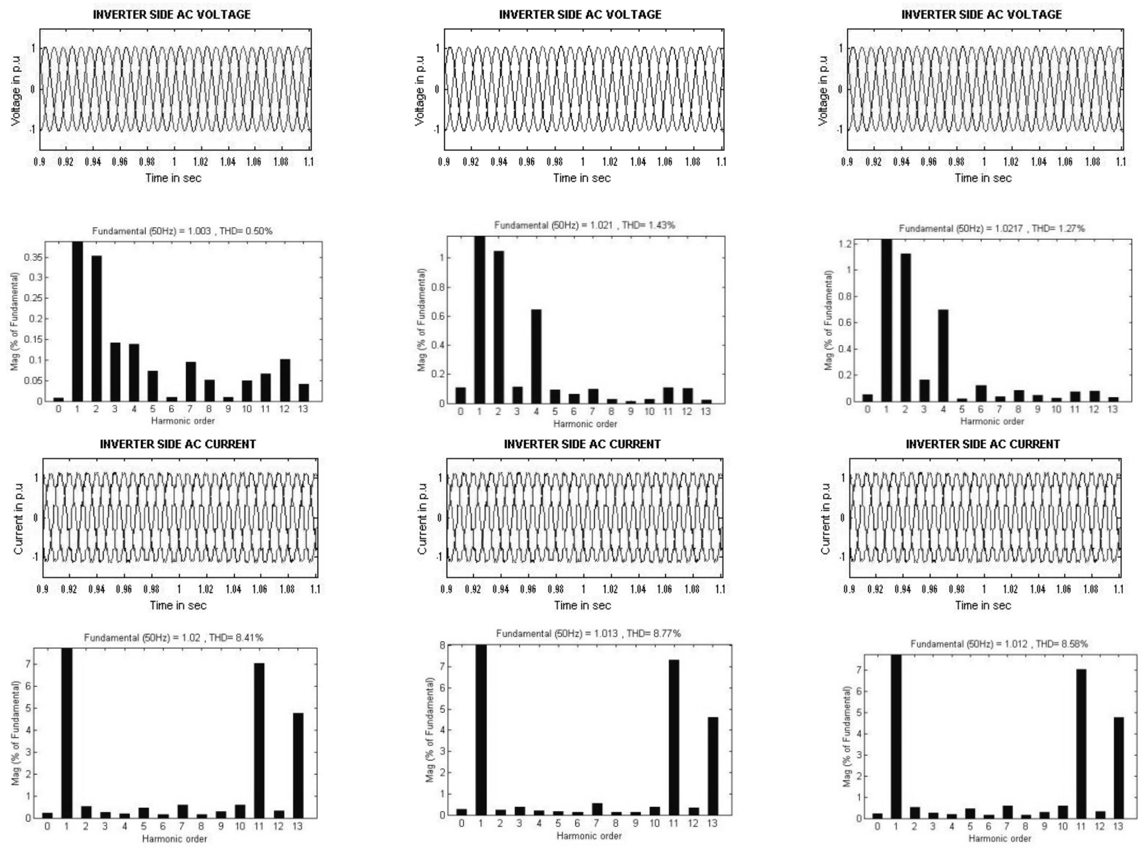

Fig. 5: Inverter side AC Waveforms and their harmonic spectrums during steady state operation - with SC (left), - with SVC (middle), -with STATCOM (right).

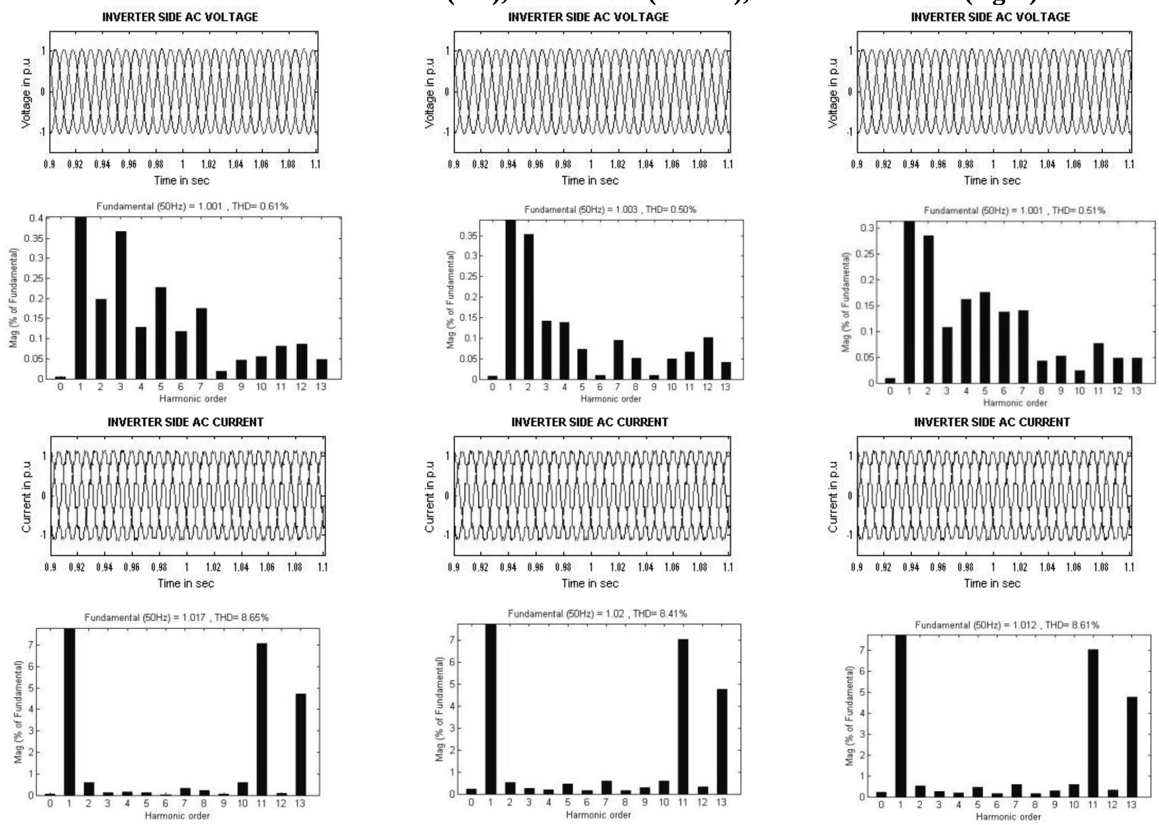

Fig. 6: Inverter side AC waveforms and their harmonic spectrums during steady state operation -with FC+SC (Left), - with FC+ SVC (Middle), -with FC+STATCOM (Right).

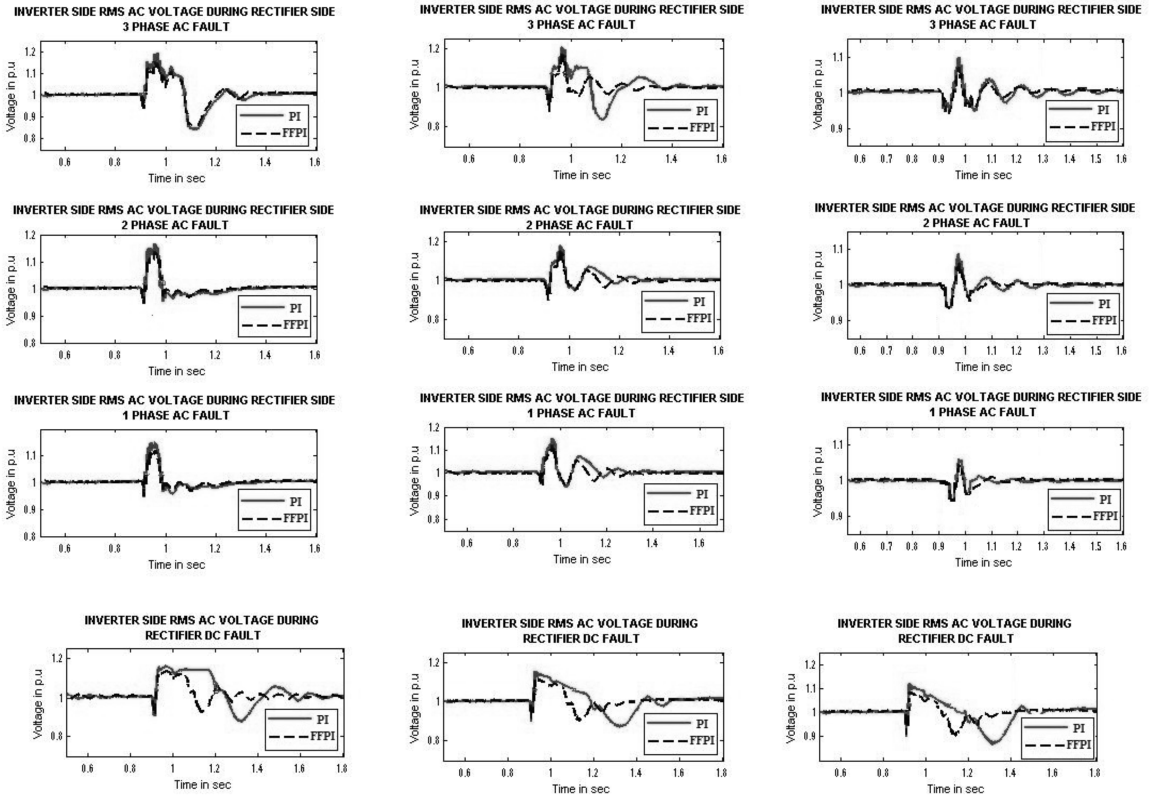

Fig. 7: Inverter AC bus RMS voltage when disturbances occur on the DC line or at the rectifier side - with SC (left), - with SVC (middle), - with STATCOM (right).

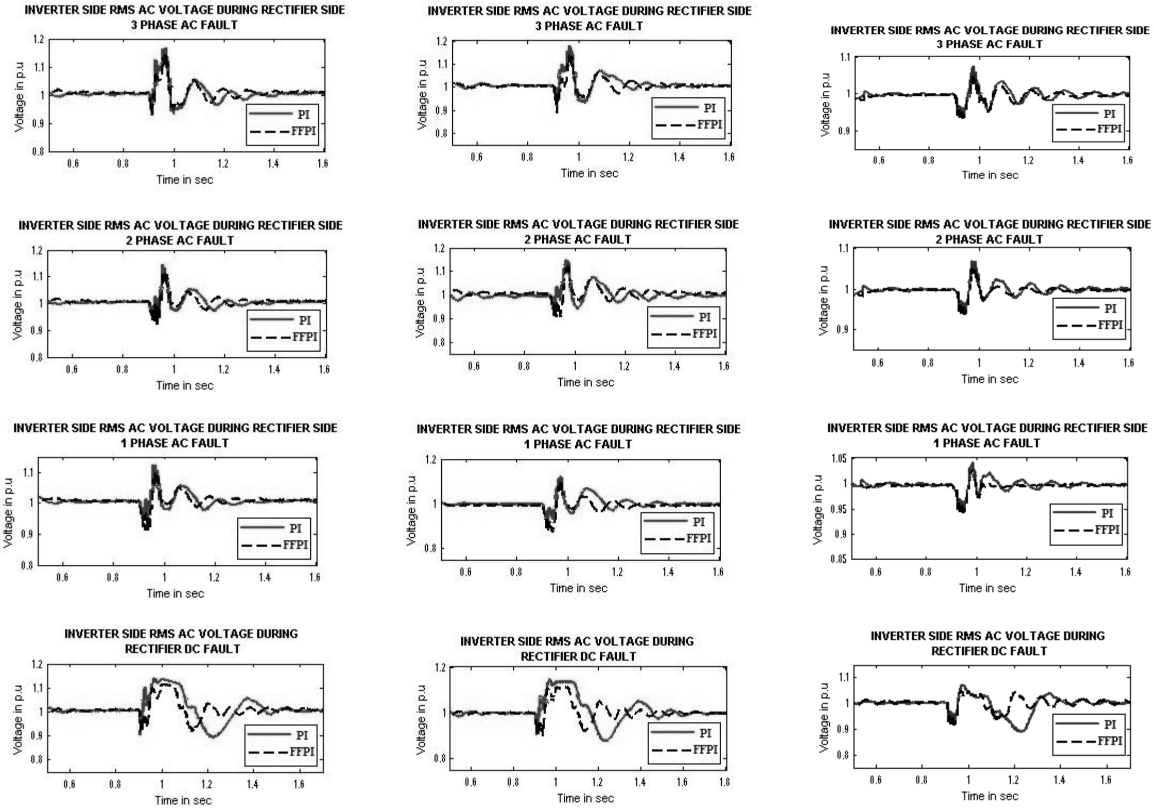

Fig. 8: Inverter AC bus RMS voltage when disturbances occur on the DC line or at the rectifier side -with FC+SC (Left), - with FC+ SVC (Middle), -with FC+STATCOM (Right).

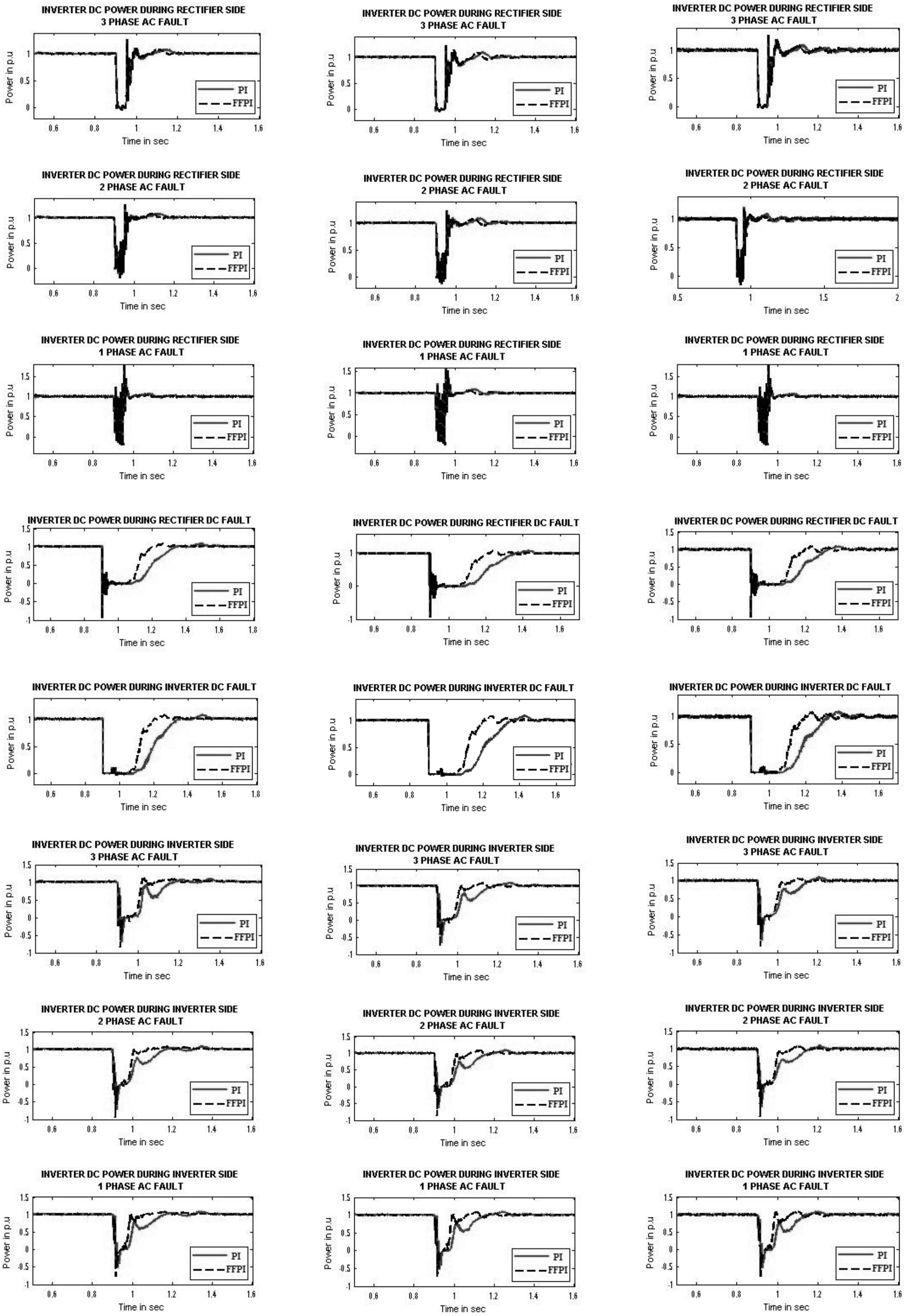

Fig. 9: Inverter DC power when AC and DC disturbances occur on the rectifier side/ the inverter side -with SC (left), -with SVC (middle), - with STATCOM (right).

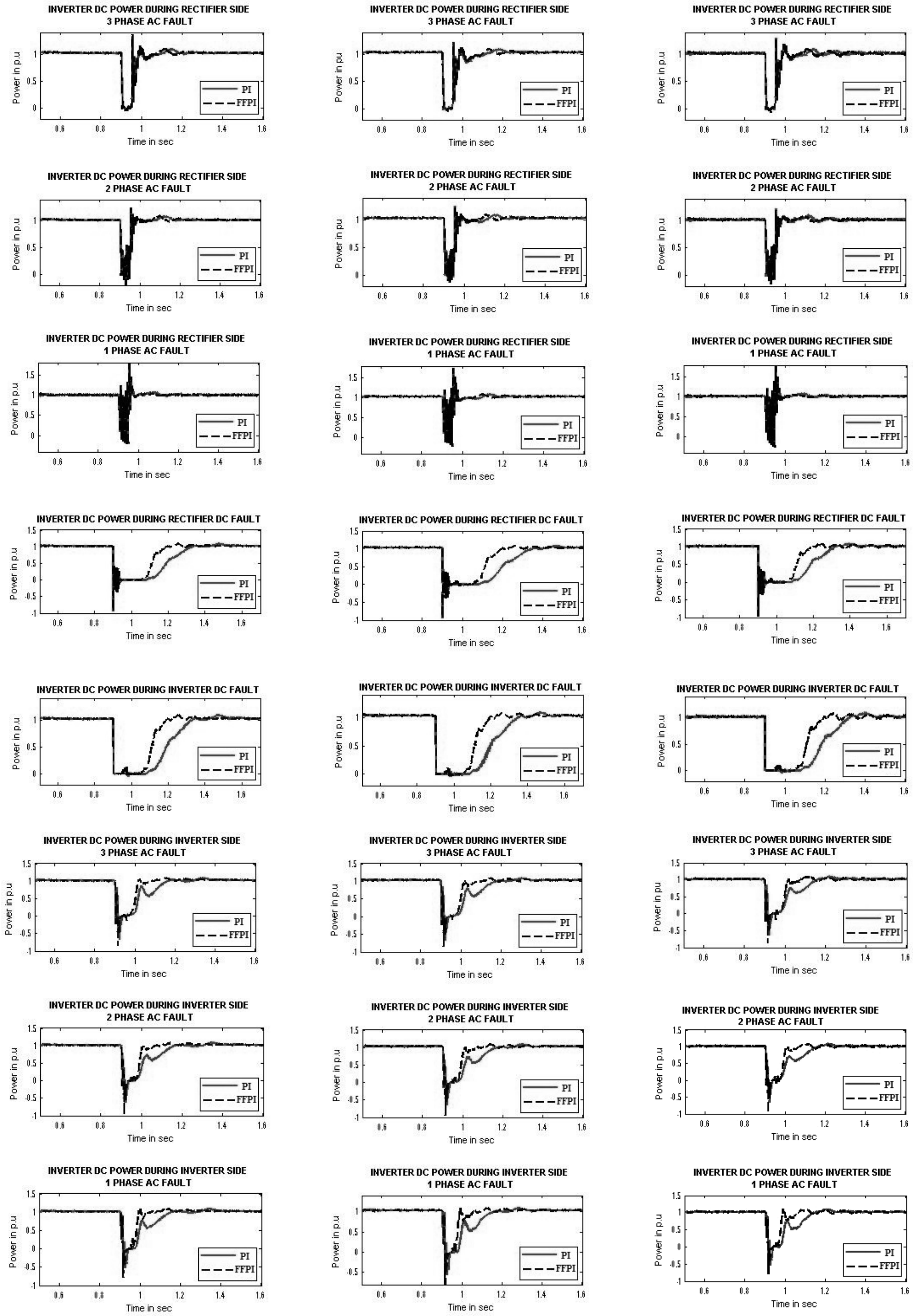

Fig. 10: Inverter DC power when AC and DC disturbances occur on the rectifier side /the inverter side -with FC+SC (Left), - with FC+ SVC (Middle), -with FC+STATCOM (Right).

Table I: Harmonics present in the inverter side AC quantities

% AC Harmonics for various RPC's	SC	SVC	STATCOM	FC+SC	FC+SVC	FC+ STATCOM
Voltage	0.50	1.43	1.27	0.61	0.50	0.58
Current	8.41	8.77	8.58	8.65	8.41	8.61

Table II: Over-voltage level when disturbances occur on the DC line or at the rectifier side during DC block

TOV for Various RPC's in p.u		Rectifier side 3Φ AC fault	Rectifier side 2Φ AC fault	Rectifier side 1Φ AC fault	Rectifier DC fault
SC	**PI**	1.1992	1.1801	1.1645	1.1588
	FFPI	1.1730	1.1504	1.1360	1.1378
SVC	**PI**	1.2131	1.1893	1.1647	1.1706
	FFPI	1.1901	1.1610	1.1379	1.1464
STATCOM	**PI**	1.1112	1.1002	1.0799	1.1087
	FFPI	1.0843	1.0764	1.0561	1.0833
FC+SC	**PI**	1.1814	1.1623	1.1421	1.1561
	FFPI	1.1599	1.1381	1.1182	1.1311
FC+SVC	**PI**	1.1920	1.1781	1.1577	1.1645
	FFPI	1.1688	1.1544	1.1328	1.1401
FC+ STATCOM	**PI**	1.0936	1.0871	1.0533	1.0821
	FFPI	1.0711	1.0622	1.0320	1.0613

Table III: Inverter DC power when AC and DC disturbances occur on the rectifier and the inverter side

DC power recovery time for Various RPC's in seconds		Rectifier side 3Φ AC fault	Rectifier side 2Φ AC fault	Rectifier side 1Φ AC fault	Rectifier DC fault	Inverter DC fault	Inverter side 3Φ AC fault	Inverter side 2Φ AC fault	Inverter side 1Φ AC fault
SC	**PI**	0.036	0.024	0.015	0.391	0.393	0.191	0.184	0.172
	FFPI	0.034	0.023	0.014	0.262	0.268	0.066	0.060	0.055
SVC	**PI**	0.037	0.025	0.016	0.406	0.407	0.196	0.191	0.180
	FFPI	0.035	0.024	0.015	0.272	0.274	0.069	0.062	0.061
STATCOM	**PI**	0.034	0.023	0.014	0.373	0.375	0.185	0.178	0.166
	FFPI	0.032	0.022	0.013	0.248	0.250	0.063	0.055	0.053
FC+SC	**PI**	0.034	0.022	0.014	0.380	0.382	0.181	0.172	0.163
	FFPI	0.032	0.021	0.013	0.251	0.253	0.061	0.056	0.051
FC+SVC	**PI**	0.035	0.024	0.015	0.394	0.396	0.186	0.179	0.170
	FFPI	0.033	0.023	0.014	0.263	0.265	0.062	0.058	0.054
FC+ STATCOM	**PI**	0.032	0.021	0.013	0.361	0.360	0.177	0.168	0.159
	FFPI	0.030	0.020	0.012	0.236	0.238	0.059	0.055	0.050

The ability of TOV suppression of various RPC's is demonstrated with the proposed firefly algorithm based PI controller and also compared to a conventional PI controller. From the inverter side RMS AC voltage waveforms shown in Fig. 7, 8 and the results listed in table II, the occurrence of TOV with the presence of a conventional PI controller for various RPC's can be understood. The hybrid RPC's (FC+SC, FC+SVC and FC+STATCOM) has improved TOV controlling capability, than their individual performance (SC, SVC, and STATCOM). In particular, FC+STATCOM have very less TOV among the various RPC's. The TOV values further reduced due to the application firefly algorithm based PI controller compared to conventional PI controller.

C.Fault Recovery

The time taken by the HVDC system to recover the 80% of the pre-fault power after the fault clearance is known as DC power recovery time. The DC power recovery time is often desired the recovery ability of a DC system PI controller and the capability of the RPC's during system disturbances. From the inverter DC power recovery simulation results (Fig. 9, 10 and table III), it is observed that in all the cases during rectifier side AC system faults, the system recovery with the firefly algorithm based PI controller is slightly faster than the conventional PI controller. On the other hand, for the faults in the rectifier DC side and inverter AC and DC side, the hybrid RPC's (SC+SVC, SC+STATCOM and SVC+STATCOM) has reduced fault clearing time than their individual performance (SC, SVC, and STATCOM). In particular, the combination of SC and STATCOM is taking very lesser time to clear the fault among the various RPC's. Further, the firefly algorithm based PI controller makes the system recovery much faster than the conventional PI controller.

V.CONCLUSION

In this paper, an in depth simulation study of a monopole LCC-HVDC system feeding a very weak AC network was carried out with hybrid RPC's and firefly algorithm based optimal PI controller for rectifier and inverter control. The various hybrid RPC's considered were FC+SC, FC+SVC and FC+STATCOM. This involvement can be very useful for designing and safeguarding persons, for analyzing the interaction between AC networks and HVDC systems under different operating environment. The HVDC transmission system model was simulated using Matlab software. The transient performances of the hybrid RPC's in an HVDC system were compared with SC, SVC, STATCOM, under various fault condition to study the suppression of TOV and fault recovery. The simulation results authenticate that the equal combination of FC+STATCOM has the steady and fastest response and display the superiority of firefly algorithm based PI controller over the conventional fixed gain PI controller. The harmonic analysis result also guarantees the quality of power supply at inverter AC side.

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