A Review on Adder Design using QCA Systolic Array

Premila S, T. Gunasekaran

Abstract—Quantum-dot cellular automata (QCA) are considered as an advanced technology compared to complimentary metal-oxide-semiconductor (CMOS) due to QCA's merits. Many logical circuits are designed using QCA which consume low power and reduced area. Therefore our interest is on designing of adders using QCA. Thus we design adders and detailed simulation using QCAD designer is presented. The performance of proposed adder gives the better Delay performance compared to Ripple carry adder (RCA).

Index terms: Quantum-dot Cellular Automata, systolic array, matrix multiplier, Galois Field multiplier, coplanar crossing, multilayer crossover.

I. INTRODUCTION

The CMOS technology has limitations such as off-state leakage and minimum fabrication dimensions. Due to these physical limitations of CMOS technology may an alternative nanotechnologies are being introduced. One promising possibility, Quantum-dot Cellular Automata QCA was introduced. There are three forms of QCA: semiconductor, molecular, and magnetic. Potential realization of semiconductor QCA design has been carried out. Cells and basic logic gates of magnetic and molecular QCA have been fabricated and tested successfully. Although QCA implementations are still in development nanotechnology promises to provide outstanding energy efficiency, high density and fast computing performance. Compare to CMOS technology, the characteristics of QCA is more interesting. In CMOS technology, carry look ahead adders are faster than ripple carry adders. In QCAs optimized layout of a 64-bit ripple carry adder is 50% faster than a 64-bit carry look ahead adder. The wire delays in QCA are problem. Since an adder is a simple component in digital circuit design, which results in extra clock cycles in QCA technology, will seriously affect the performance of a QCA system. Therefore this paper investigates more complex architectures based on semiconductor. QCA, focus on logic Level QCA circuit design, to explore the characteristics of QCA technology. To increase the performance of a computing system, systolic array architectures, were introduced. These involve an arrangement of processors in an array where data flow synchronously across the array between neighbours. Each processor takes input data from neighbours, processes them and gives the results. Processors in the array compute data and store them independently.

In this pipelined manner, systolic arrays can be very fast and easily scalable in comparison to single processor machines. In this pipelined manner, data flow control becomes easy. Therefore the cost in control signal generation or finite state machine (FSM) design is significantly reduced. They are highly specialized; systolic arrays are widely used in signal processing, image processing, graphic algorithms, biological sequence comparison.

II. QCA BASICS

QCA is based on the interface of bi-stable QCA cells constructed from four quantum-dots. A high-level design of two polarized QCA cells is shown in Fig. 1. Each cell is constructed from four quantum dots arranged in a square pattern. The cell is charged with two electrons, which are free of charge to tunnel between adjacent dots. These electrons tend to take up antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equal energetically minimal arrangements of the two electrons in the QCA cell as shown in Fig. 2. These two arrangements are denoted as cell polarization $P = +1$ and $P = -1$ correspondingly. By using cell polarization $P = +1$ to represent logic "1" and $P = -1$ to represent logic "0", binary information can be encoded.
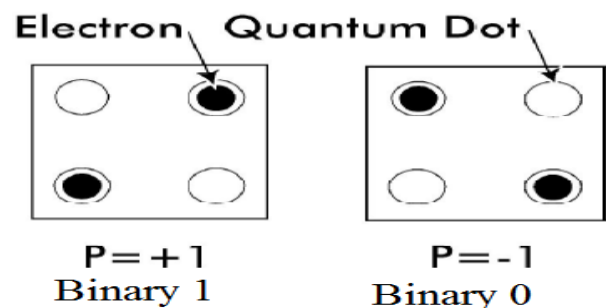

Fig. 1 Basic QCA cells

Arrays of QCA cells can be set to perform all logic functions. This is owed to the Columbic interactions, which influences the polarization of neighbouring cells. QCA designs have been proposed with potential barriers between the dots that can be controlled and used to clock QCA designs. The fundamental QCA logic devices are the QCA wire, majority gate and inverter. QCA wire: In a QCA wire, the binary signal propagates from input to output because of the Columbic connections between cells. This is a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a high energy level, and would soon settle to the correct ground state. The propagation in a 90-degree QCA wire is shown in Fig. 2. Other than the 90- degree QCA wire,

a 45-dgree QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations. Advance, there exists a so called non-linear QCA wire, in which cells with 90-degree orientation can be placed next to one more ,but off centre.
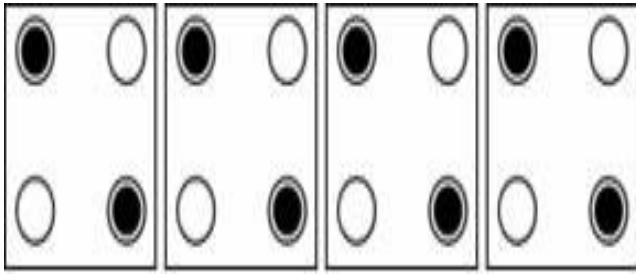

Fig. 2 A wire of quantum-dot cells

Majority gate and inverter: The majority gate and inverter are shown in Fig. 4 and Fig. 5 respectively. The majority gate performs a three-input logic function. Assuming the inputs are A, B and C, the logic function of the majority gate is

$$m(A, B,C) = A|B + B|C + A|C$$

By fixing the polarization of one input as logic "1" or "0", we can get an OR gate and an AND gate respectively. More complex logic circuits can then be designed from OR and AND gates.
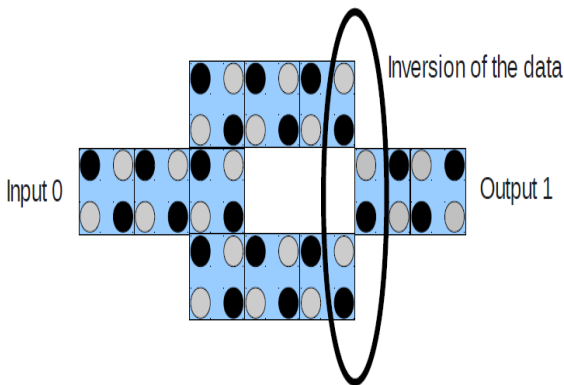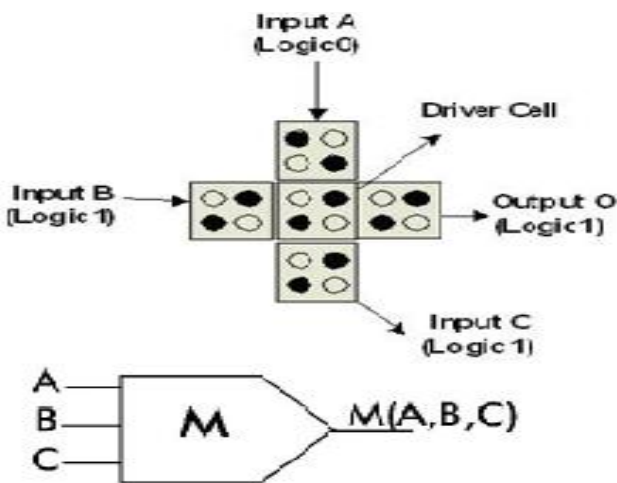

Fig. 3 A QCA inverter
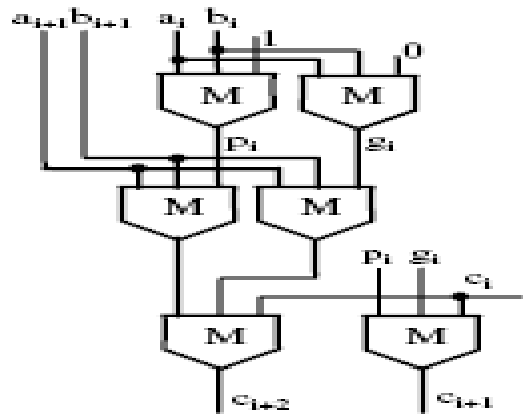

Fig. 4 A QCA majority gate

Fig. 5 Novel QCA Full Adder

III. PROPOSED METHOD

A QCA is a nano-structure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots inside the cell. Because of Coulombic repulsion, the two electrons will forever reside in opposite corners. The locations of the electrons in the cell determine two possible stable states that can be associated to the binary state 1 and 0. Although adjacent cells interact through electrostatic forces and tend to arrange in a line their polarizations, QCA cells do not have intrinsic data flow directionality. To achieve controllable data directions, the cells inside a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock system named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch. QCA cells are used for both logic designs and interconnections that can exploit either the coplanar cross or bridge technique. The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs a, b, and c, the MG perform the logic function reported in (1) provided that all input cells are associated to the same clock signal clk x (with x ranging from 0 to 3), whereas the $p\square = a\square + b\square$ and $g\square = a. b$, are compute for each bit of the operands and then they are grouped four by four.
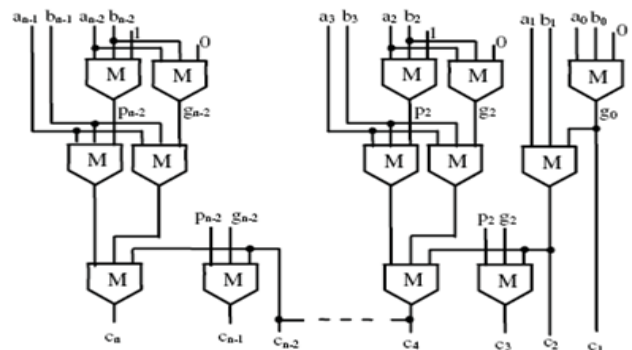

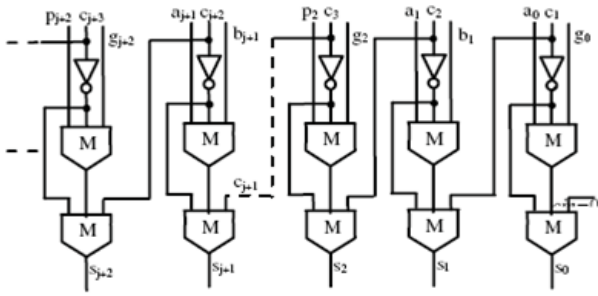**Fig. 6 Novel n-bit adder -carry chain**

Fig. 7 Sum block

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and suppose that for the *i* th bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $p_i = a_i + b_i$ and $g_i = a_i \cdot b_i$, are computed. C_i being the carry produced at the generic $(i-1)$th bit position, the carry signal c_i+2, furnished at the $(i+1)$th bit position, can be computed using the conventional CLA logic reported in (2). The latter can be rewritten as given in (3), by exploiting Theorems 1 and 2 demonstrated in [15]. In this way, the RCA action, needed to propagate the carry c_i through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA. Equation (3) is exploited in the design of the novel 2-bitmodule shown in Fig. 1 that also shows the computation of the carry $c_i+1 = M(p_i \; g_i c_i)$. The proposed *n*-bit adder is then implemented by cascading $n/2$ 2-bit modules as shown inFig.4.2.a. Having assumed that the carry-in of the adder is $cin = 0$, the signal p_0 is not required and the 2-bit module used at the least significant bit position is simplified. The sumbits are finally computed as shown in Fig. 4.2.b.It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position(i.e., $g_0 = 1$) and then it is propagated through the subsequent bit positions to the most significant one.
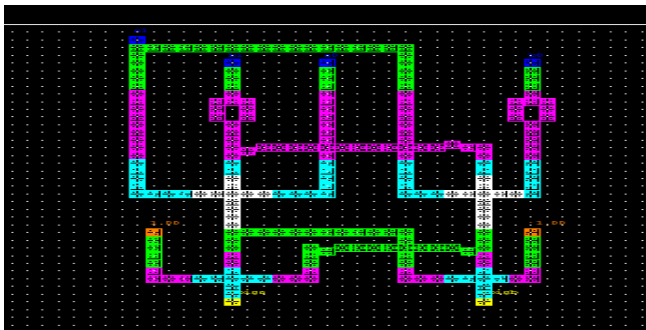

Fig. 7 Adder Layout

In this case, the first2-bit module computes c_2, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bitmodules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to $(n - 2)/2$. Considering that further two MGs and one inverter are required to compute the sum bits, the worst

case path of the novel adder consists of $(n/2) + 3$ MGs and one inverter

$$ci+2 = g_{i+1} + p_{i+1} \cdot g_i + p_{i+1} \cdot p_i \cdot c_i$$
$$ci+2 = M(M(a_{i+1}, b_{i+1}, g_i) \, M(a_{i+1}, b_{i+1}, p_i) \, c_i)$$
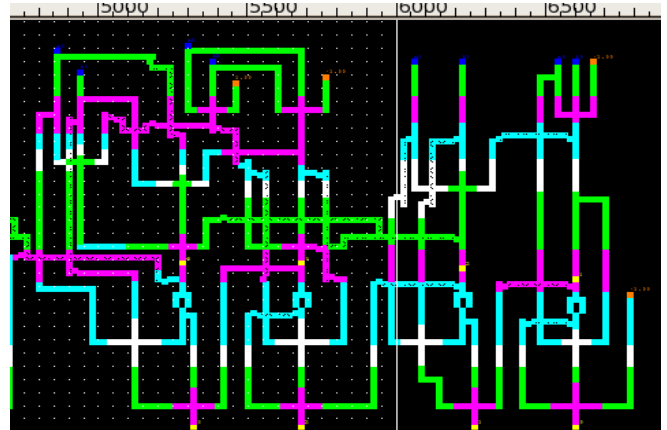

Fig. 8 QCA layout of 16-bit adder

The proposed addition architecture is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings. The QCA cells are 18-nm wide and 18-nm high; the cells are placed on a grid with a cell center-to-center distance of 20 nm; there is at least one cell spacing between adjacent wires; the quantum-dot diameter is 5 nm; the multilayer wire crossing structure is exploited; a maximum of 16 cascaded cells and a minimum of two cascaded cells per clock zone are assumed. The coherence vector engine is used for simulations.

IV. RESULTS

The proposed addition design is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings used.
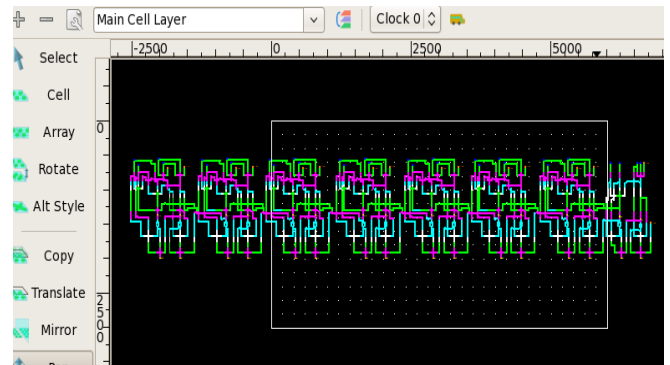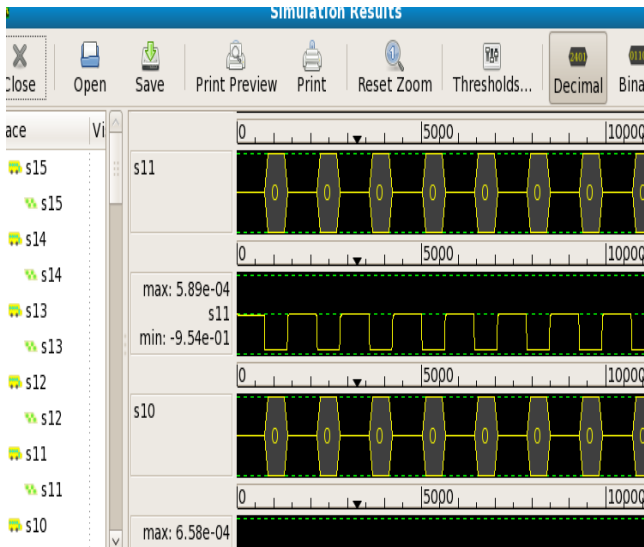

Fig. 9 QCA Layout

Fig. 10 Output Vector

V. CONCLUSION

A new adder designed in QCA was implemented. It achieved speed performances high than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lesser than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited.

REFERENCES

1. Liang Lu, Weiqiang Liu,Ma´ ire O'Neill, and Earl E. Swartzlander Jr. "QCA Systolic Array Design," vol no 62,march 2013.
2. C. Lent,B. Isaksen, and M. Lieberman, "Molecular Quantum-Dot Cellular Automata," J. Am. Chemical Soc., vol. 125, pp. 1056-1063, 2011.
3. I. Amlani, A. Orlov, G. Toth, G. Bernstein, C. Lent, and G. Snider, "Digital Logic Gate Using Quantum-Dot Cellular Automata," Science, vol. 284, pp. 289-291, 2011.
4. X. Ma, J. Huang, and F. Lombardi, "A Model for Computing and Energy Dissipation of Molecular QCA Devices and Circuits," ACM J. Emerging Technologies in Computing Systems, vol. 3, pp. 1-30, 2010.
5. A.DeHon and M. Wilson, "Nanowire-Based Sublithographic Programmable Logic Arrays," Proc. ACM/SIGDA 12th Int'l Symp. Field Programmable Gate Arrays, pp. 123-132, 2009.