Design D Flip-Flop for Low Power Application

Kumar Vinayak, Owais Ahmad

Abstract: ***Power consumption is a major problem of system performance and it is listed as one of the top three challenges in International Technology for Semiconductor. In practice, a large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. In this thesis, various design techniques for a low power clocking system are surveyed. Among them minimizing a number of clocked transistor is an effective way to reduce capacity of the clock load. To approach this, we propose a conditional data mapping technique which reduces the number of local clocked transistors.***

Keywords: Flip Flop, Low Power, CMOS Circuit

I. INTRODUCTION

PROPOSED WORK

1.1 Theoretical design procedure

This chapter will discuss on a proposed new clocked pair shared d flip-flop design The proposed work aims to study the various possible methods of CPSDFF and to assess the low power consumption various techniques. In the present work, .In contrast, flip-flop (CPSDFF), reduction in the number of clocked transistors the objective to reduce clocked load our study CDFF and CCFF use many clocked transistors, CDMFF reduces the number of clocked transistors but it has redundant clocking as well as a floating node. To ensure efficient and robust implementation of low power sequential element, we propose CPSDFF (fig 1.1) to use less clocked transistor than CDMFF and over-come the floating problem in CDMFF

1.2 Circuit description

In this circuit of clocked-pair-shared flip-flop, a clocked pair (N3, N4) is shared by first and second stage of the latching part as which is shown in figure 1.1 clocked loads which is used in CDMFF, it result in about 40% reduction in number of clocked loads. Additional to this the internal node X is connected to supply voltage Vdd with the help of a pseudo NMOS P1, so is not floating point is now present, and result also shows an improvement in the noise robustness of node X.

When input D stays at HIGH level then Q=1, here N5 is kept ON, N1 will be kept off to avoid the redundant transient activity at node X, as well as in any short circuit current. PMOS P2 is allowed to pull Q to high level when D switches to 1 value. Then second NMOS branch (N2) is in charge for pulling down the output of Q if D = LOW value and Y=1when the clock pulse is arrives. PMOS present in N1 should turn on NMOS N2 when D=LOW.

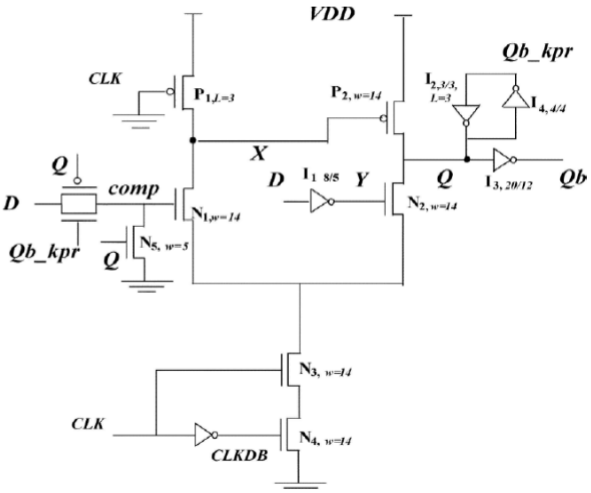

Figure 1.1 Diagram of CPSDFF

Although P1 is always ON, short circuit only occurs one time when D makes a transition from LOW to HIGH, and then discharge path is disconnected after two gates delay. After all that, if at this time also D remains at HIGH, then the discharge path is already disconnected by N1; there would be no short circuit. Here the clocked-pseudo-NMOS scheme is different from the general idea of common pseudo-NMOS logic. In the previous one we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly scaled to guarantee a correct noise margin. CPSFF uses three less clocked loads, which by default leads to about 40% reduction in number of clocked loads. It achieves 25% less clock driving power consumption than CDMFF, which improves power efficiency.

II. METHODOLOGY

1.1. Surveyed technique for reducing clock

Most of the flip-flops presented here are dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose. A brief survey of such techniques is conducted in this work, and the main techniques were classified as follows: Reducing Capacity of Clock Load: 80% of non clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity in equation.

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In my project I am making a comparison (power) with the existing flip flop and find out that the new flip flop reduces the power. CPSDFF use less clocked transistor than CDMFF, CDFF&CCFF overcome the floating problem.

Advantages

- CPSDFF uses less clocked Transistors
- Less power & Area
- very less clock delay

III. RESULT AND DISCUSSION

3.1. Simulation results of proposed CPSDFF

All the simulation results which include sizing of transistors, power consumption and timing metrics are obtained and discussed in this chapter The performance of the proposed CPSDFF was verified using the PSpice simulation program The simulation results flip flop were obtained from P-SPICE simulation in 0.18µm CMOS technology at room temperature ,the supply voltage is 1.8v. The aspect ratio of the transistor are given in Table 2.1.The parasitic capacitances were extracted from the layouts. The setup used in our simulation is shown in Fig.2.1-In order to obtain accurate results .we have simulated the circuits in a real environment, where the flip flop inputs(clock, data) are driven by the buffers, and the output is required to drive an output load. An inventor is placed after output Q, providing Protection from direct noise coupling. The value of the capacitance load at Q_b is 10fF, which is selected to simulation a fan out of 14 minimum sized invertors (FO14). A clock frequency of 111MHz is used. The results of the CDMFF circuit show 10.276µW power dissipation. Flip flop with reduced number of transistor for low power &high performance

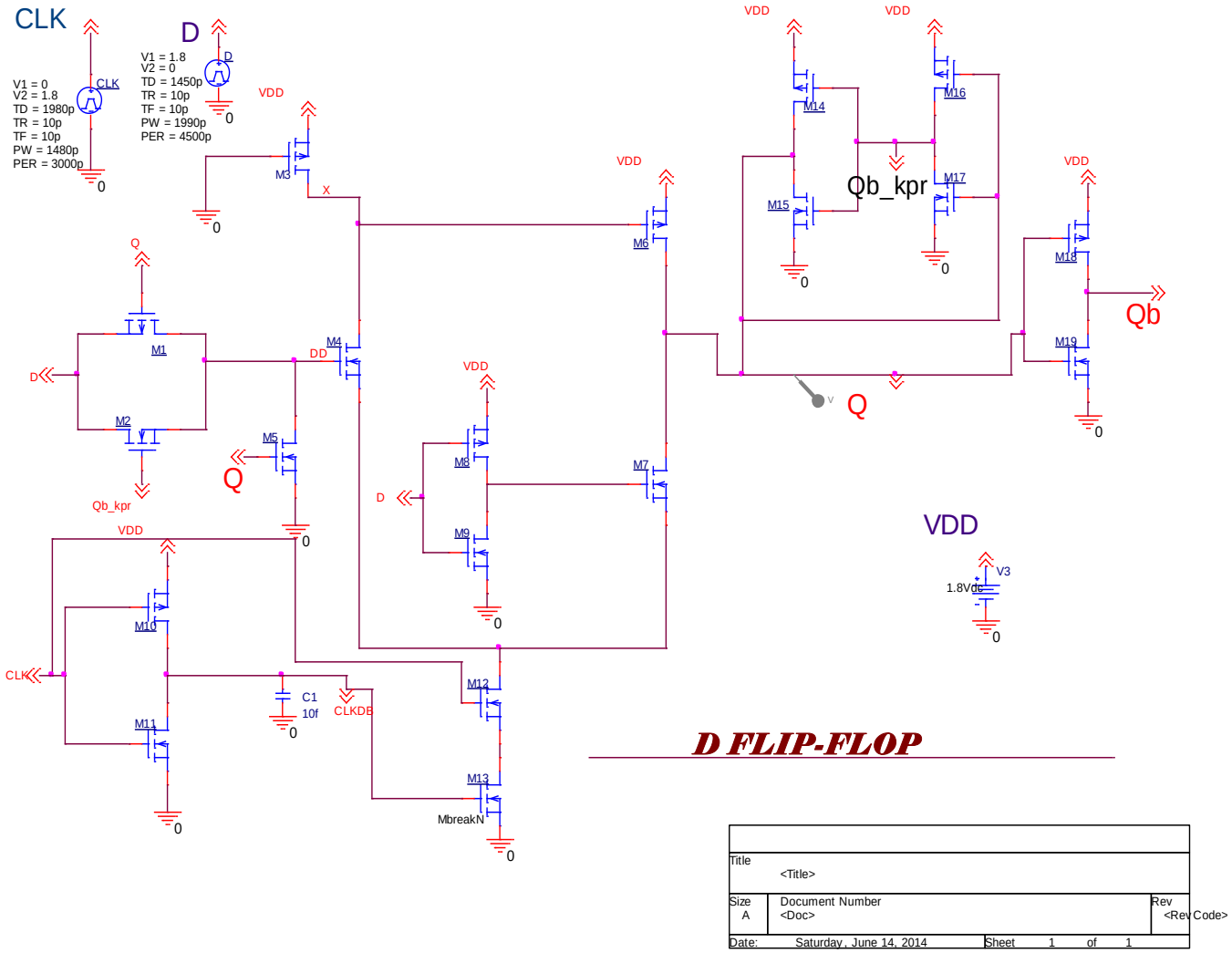

Fig 2.1:- PSPICE capture of CPSDFF

Table 2.1 Aspect ratios of the transistors CPSDFF

A test bench is setup to compare the performance of all flip-flops as shown in Figure

Transistor	W(μm)	L(μm)
M1,M2,,M4	2.25	0.18
M3	5	3
M5	0.9	0.18
M6,M7,M12,M13	2.52	0.18
M8,M9	8	5
M10,M11,M14,M15	3	3
M16,M17	4	4
M18,M19	20	12

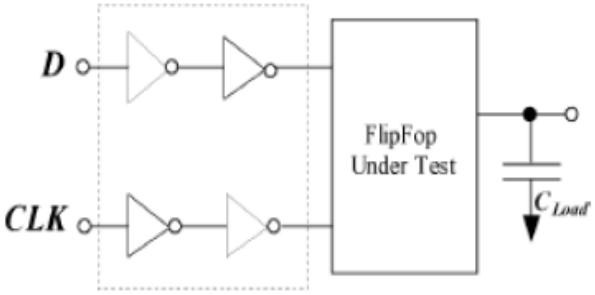

Fig 2.2 Setup used for flip flop simulation the Input are driven by the inverters, and output is driving a capacity load of14 minimum inverters(FO14)

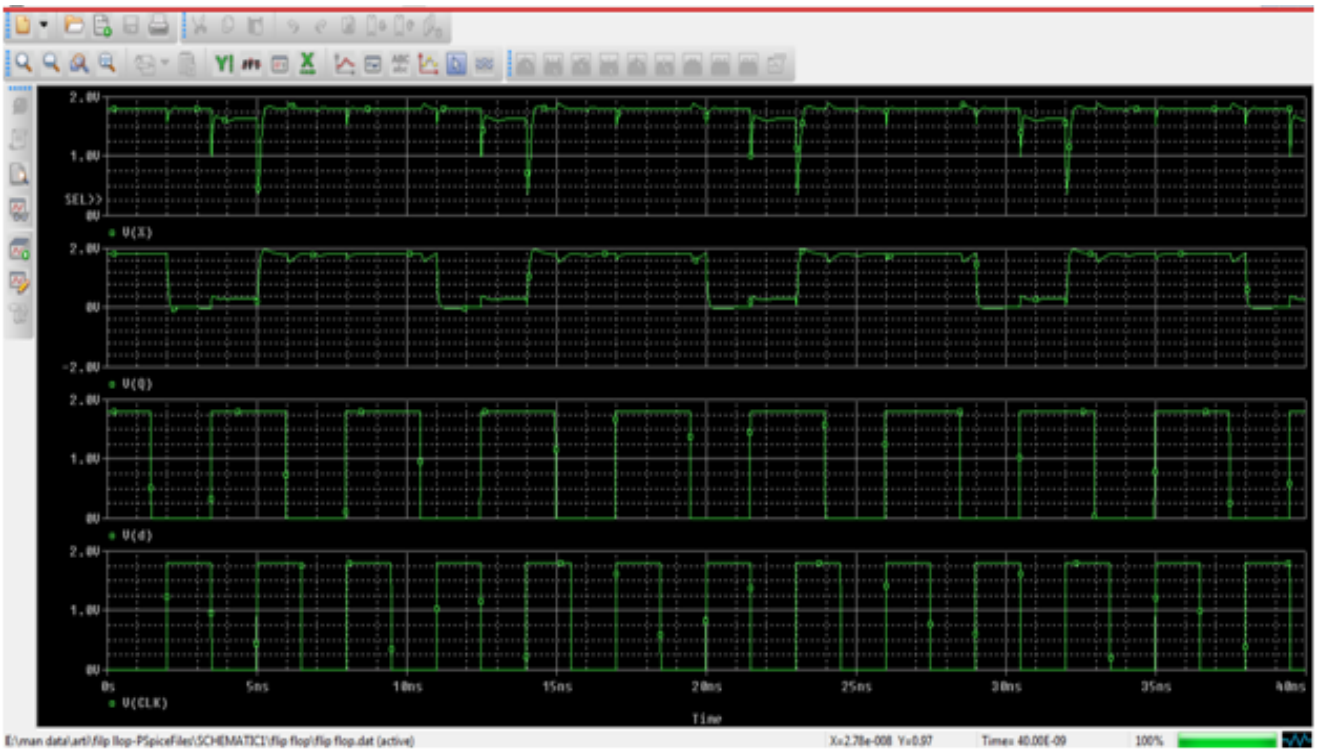

Figure 2.3:-Simulation result of CPSDSFF

Fig 2.3 shows the output voltage with respect to clock in work on D flip flop while X and Y terminal are terminated with 2.0v to 40 ns

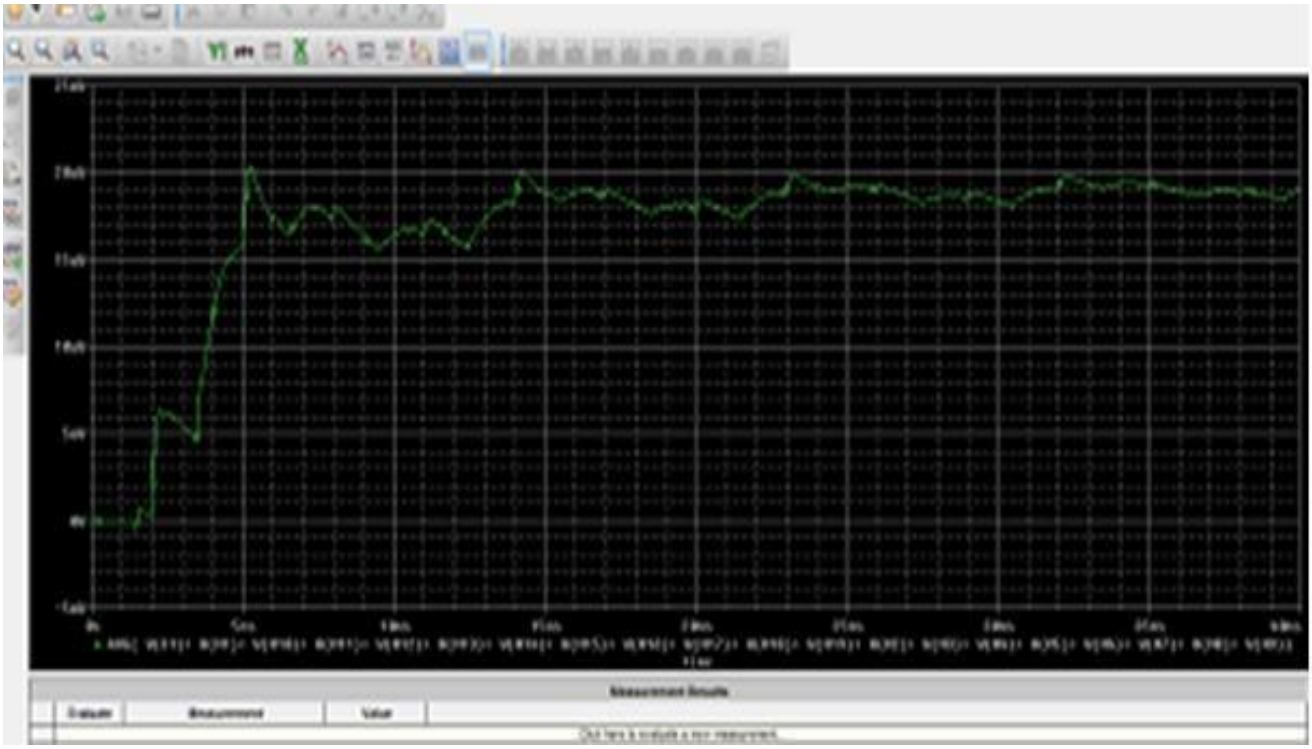

Fig2.4:- Waveform for Power Consumption at process

Fig 2.4 shows the Average power dissipation with respect to time in work on D flip flop while X and Y terminal are terminated with 20uw to 40 ns respectively .The total power dissipation is 10.276µ watts.

Comparison of Total Power dissipation table:-

TYPE	NO of Transistor	No of Clocked	Power Consumption
CDMFF	22	7	11.253µw
CPSDFF	14	4	10.276µw

The results of the CPSDFF circuit show 10.276 W power dissipation. Flip flop with reduced number of transistor & reduction in size by reducing the number of clocked load for low power &high performance.

IV. CONCLUSION

In this project, a variety of design techniques for low power clocking system are reviewed. One effective method, reducing capacity of the clock load by minimizing number of clocked transistor, is elaborated. Following the approach, one novel CPSDFF is proposed, which reduces local clock transistor number by about 40%. In view of power consumption of clock driver, the new CPSDFF outperforms prior arts in flip-flop design by about 24%.In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits. Our experimental results enabled us to identify the power and performance trade-offs of the flip-flop design. The simulation environment is setup with a supply voltage of 1.8V, temperature, clock frequency of 111 MHz and a capacitive load of 10fF.

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