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Enhancement of Power Quality for 15 Level Inverter using Phase Disposition-PWM Technique

Richa Gupta

Abstract*: With consideration of use of solar, wind and other renewable energy source for industrial applications like electric vehicle drive, train traction and FACTS integration, which demand voltage levels in the range of kilo volts with high power quality, to achieve this high voltage level and high quality of power, a cascaded H-bridge multilevel inverter based topology capable of operating with low harmonic distortion is proposed in the paper. In order to attain low total harmonic distortion (THD), use of phase disposition-PWM technique is proposed in the paper. Giving due attention to both switch count and low THD, the output voltage levels of the multi-level inverter are set at 15 levels. Due to half wave symmetry the even order harmonics for proposed system become zero and the lower order harmonics reduces which is shown in tabular from. Due to reduced switch count and low THD the overall system become more efficient and effective. The effectiveness of the proposed control strategy has been verified using MATLAB simulations. Simulation is done for both symmetrical as well as asymmetrical multilevel inverter topology. It is observed that quality of the output voltage waveforms of the multi-level inverter (MLI) is as per the IEEE std 519 specifications. For symmetrical reduced switch fifteen level inverter the THD is 4.42% and for asymmetrical topology THD is 4.59% for the output voltage waveform.

Keywords*: Multi-level inverter (MLI), Total harmonic distortion (THD), Pulse width modulation (PWM), Phase Disposition (PD).

I. INTRODUCTION

Owing to the deteriorating environmental conditions and diminishing energy resources, the recent research trend has been focusing towards the enhanced use of renewable energy sources. In this regard, solar and wind energy based applications have been the favorite topics in the field of power electronics [1]. With limited voltage levels available for the switching devices like IGBT and Thyristors, one of the major concerns in the field of solar energy have been the high voltage (HV) applications like electric vehicle drive (400V-800V), train traction (66kV-132kV) and FACTS integration (500kV-700kV). Multilevel inverters have come up as an overriding solution for such high power and medium voltage energy operations [2]. The vital concern with the multilevel inverters is topology, power quality and control operations. Diode clamped, Flying-capacitor and cascaded multi-level inverter are among the three most popular topologies for HV applications [3]. Among these, cascaded multilevel inverters have been the most popular ones due to their modular structure. Also, extra components like capacitors and diodes become inessential. The most important feature required from the MLI is high quality of output voltage waveform [10] and reduced *dv/dt* stress. Operation can done at both fundamental as well as high switching frequency. With odd number of voltage level it has been observed that will generate zero common mode voltage. Electromagnetic interference reduced [10]. Irrespective of the topology, generation of such high voltage levels is an issue in terms of power quality. Apart from that reliability issues due to high number of switches are also a major concern which require due consideration. In recent decades many conventional methods have been used to solve these above problems. Methods such as space vector modulation (SVPWM) [9], carrier based GA-SHE [8], carrier phase shift pulse width modulation (CPS-PWM) [7], sinusoidal pulse width modulation (SPWM) [5], phase shift pulse width modulation (PS-PWM) [6], selective harmonic elimination pulse width modulation (SHE-PWM)[6], pulse width modulation (PWM) [5] are the major trends of recent times. The major focus of all these techniques is the betterment and improvement of the fundamental output voltage, hence reduction of the total harmonic distortion. The reduced switch topology proposed by Rohit Kumar et al. [4] has been considered and a phase disposition PWM (PD-PWM) technique is proposed for the reduction of harmonics.

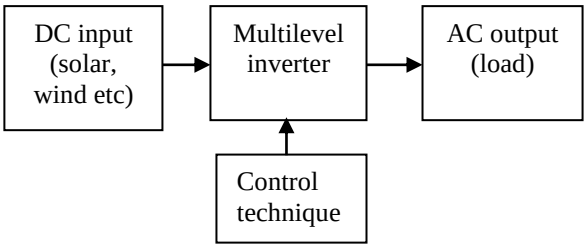

Fig. 1. Simple block diagram [2]

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Single phase of *m*-level cascaded H-bridge inverter is shown in Fig. 2. The input side comprises of independent dc sources while the output side of the inverter is connected in series for voltage amplification. The input side dc voltage can be obtained through the use of combination of solar panels, wind , fuel cell, batteries etc. Each H-bridge unit generates a quasi square wave.

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* Correspondence Author
Richa Gupta*, Research Scholar, Electrical Engineering Department, SGSITS, Indore(M.P.), India. Email: richa.science111@gmail.com

The output of inverter is almost sinusoidal with each of H-bridge addition as the voltage level increases but the requirement of switch also increases. On taking this point into consideration reduced switch topologies become a major concern for better results.

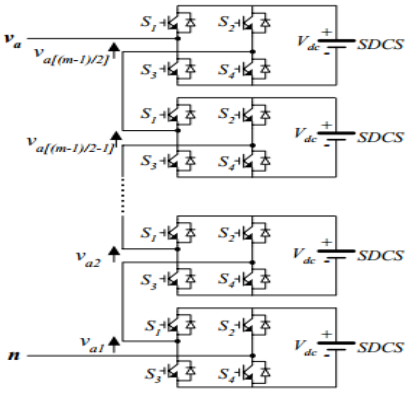


Fig. 2. Single phase H-bridge inverter[11]

III. REDUCED SWITCH TOPOLOGY

This topology is proposed [4] shown in fig. 3. This topology works for both symmetrical as well as asymmetrical input voltage levels. This topology has been divided into two stages one is level generator and another is polarity generator. Level generator uses seven switches Sw1, Sw2, Sw3, Sw4, Sw5, Sw6, Sw7 to produce 15 level. Polarity generator uses four switches T1, T2, T3 & T4 for the production of bipolar output voltage.. The conventional topology for cascaded MLI converted into reduced switch topology due this switching losses reduced and the system become more efficient.

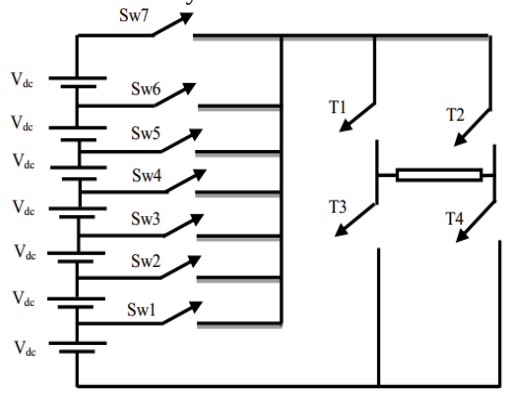


Fig. 3. 15 level 11 switch topology[4]

Table- I: Switching states of Reduced switch topology

State	Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7
0	0	0	0	0	0	0	0
V_{dc}	1	0	0	0	0	0	0
$2V_{dc}$	0	1	0	0	0	0	0
$3V_{dc}$	0	0	1	0	0	0	0
$4V_{dc}$	0	0	0	1	0	0	0
$5V_{dc}$	0	0	0	0	1	0	0
$6V_{dc}$	0	0	0	0	0	1	0
$7V_{dc}$	0	0	0	0	0	0	1

Seven +ve and seven -ve and a zero voltage level are generated by polarity generator having 1 H-bridge consist of four switches T1, T2, T3 and T4. Table 1 shows the on and off state of IGBT. '1' indicate on state and '0' indicate off state.

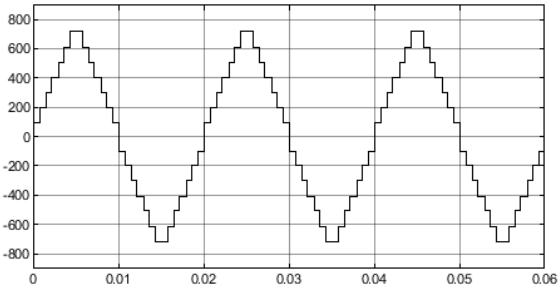


Fig. 4. Simulation result for 15 level output voltage waveforms with switching states

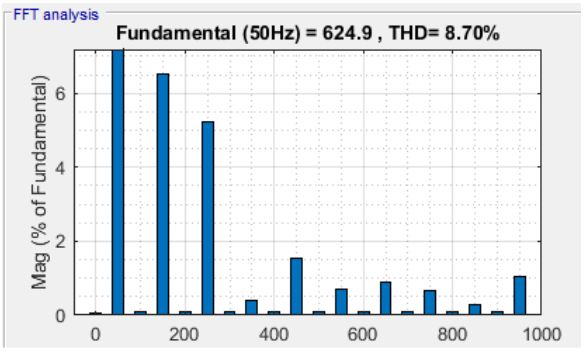
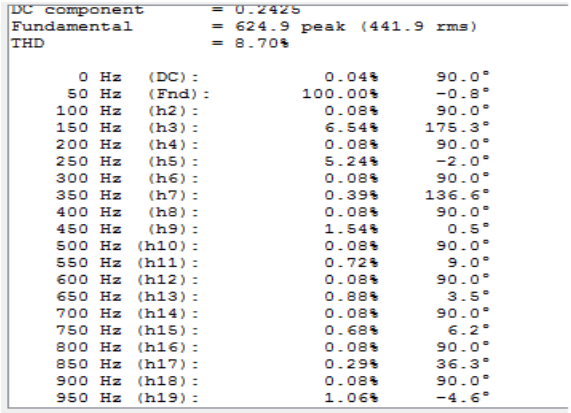


Fig. 5. FFT analysis for Symmetric MLI with switching states



```
DC component      = 0.2425
Fundamental       = 624.9 peak (441.9 rms)
THD               = 8.70%

     0 Hz   (DC):          0.04%     90.0°
    50 Hz   (Fnd):       100.00%     -0.8°
   100 Hz   (h2):          0.08%     90.0°
   150 Hz   (h3):          6.54%    175.3°
   200 Hz   (h4):          0.08%     90.0°
   250 Hz   (h5):          5.24%     -2.0°
   300 Hz   (h6):          0.08%     90.0°
   350 Hz   (h7):          0.39%    136.6°
   400 Hz   (h8):          0.08%     90.0°
   450 Hz   (h9):          1.54%      0.5°
   500 Hz  (h10):          0.08%     90.0°
   550 Hz  (h11):          0.72%      9.0°
   600 Hz  (h12):          0.08%     90.0°
   650 Hz  (h13):          0.88%      3.5°
   700 Hz  (h14):          0.08%     90.0°
   750 Hz  (h15):          0.68%      6.2°
   800 Hz  (h16):          0.08%     90.0°
   850 Hz  (h17):          0.29%     36.3°
   900 Hz  (h18):          0.08%     90.0°
   950 Hz  (h19):          1.06%     -4.6°
```

Fig. 6. FFT analysis in list view for Symmetric MLI with switching states

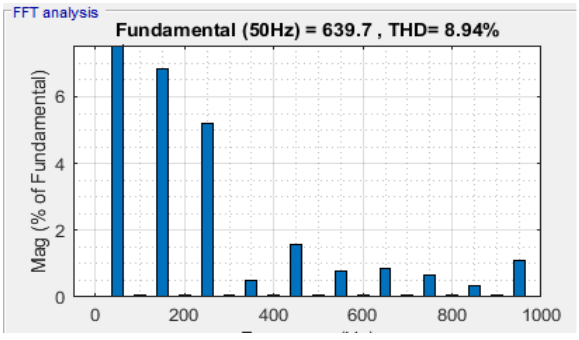


Fig. 7. FFT analysis for asymmetric MLI with switching states

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DC component      = 0.246
Fundamental       = 639.7 peak (452.3 rms)
THD               = 8.94%

      0 Hz   (DC):          0.04%     90.0°
     50 Hz  (Fnd):        100.00%     -0.8°
    100 Hz   (h2):          0.08%     90.0°
    150 Hz   (h3):          6.85%    175.4°
    200 Hz   (h4):          0.08%     90.0°
    250 Hz   (h5):          5.21%     -2.0°
    300 Hz   (h6):          0.08%     90.0°
    350 Hz   (h7):          0.51%    146.9°
    400 Hz   (h8):          0.08%     90.0°
    450 Hz   (h9):          1.58%      0.2°
    500 Hz  (h10):          0.08%     90.0°
    550 Hz  (h11):          0.79%      7.0°
    600 Hz  (h12):          0.08%     90.0°
    650 Hz  (h13):          0.86%      3.8°
    700 Hz  (h14):          0.08%     90.0°
    750 Hz  (h15):          0.66%      6.7°
    800 Hz  (h16):          0.08%     90.0°
    850 Hz  (h17):          0.32%     29.4°
    900 Hz  (h18):          0.08%     90.0°
    950 Hz  (h19):          1.08%     -4.9°
```

Fig. 8. FFT analysis in list view for asymmetric MLI with switching states

Fig. 4 shows the simulation result for output voltage of reduced topology of 15 level cascaded H-bridge inverter without PD-PWM. Fig. 5 to 8 shows the FFT analysis. In which the THD for symmetric MLI is 8.70% and for asymmetric MLI is 8.94%. To reduce the harmonic distortion PD-PWM technique is applied and a system is proposed which has better and effective results.

IV. MODULATION TECHNIQUE

Phase Disposition Pulse Width Modulation(PD-PWM)

This is a sinusoidal pulse width modulation technique (SPWM)[13]. In this technique all the carrier signals are in phase and shifted by levels. In fig.9 shows the principle of pulse generation for single level PD-PWM. The carrier signals are V_{c1} and V_{c2} while the reference signal is V_r . comparison of these two carrier signals with the reference signal is done which generates the pulses which has to be given to the corresponding switches.

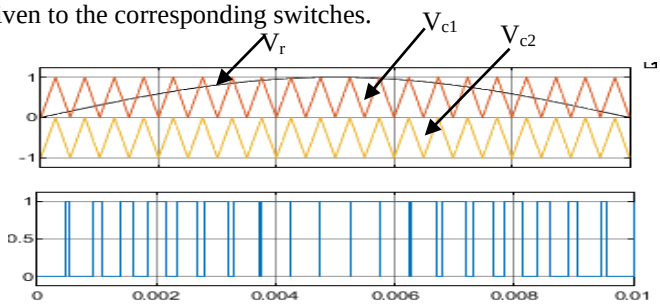


Fig. 9. Simulation result for PD-PWM pulse generation for single level H- bridge inverter

V. FLOWCHART

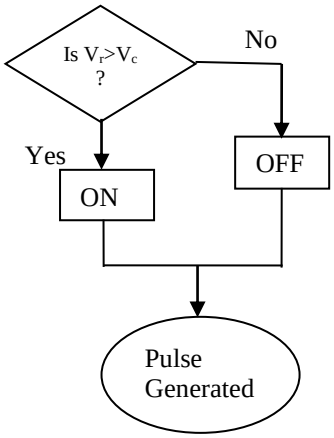


Fig. 10. Flowchart for pulse generation

VI. PROPOSED PD-PWM TECHNIQUE FOR REDUCED SWITCH TOPOLOGY

Various type of modulation technique have been proposed for MLI [5]. In this proposed topology IGBT used as switch because of their power handling capability and simple gate drive circuit. Multicarrier based sinusoidal PWM has been used with carrier frequency 2k Hz. A sinusoidal waveform of 50 Hz as a reference signal and carrier wave of 2k Hz has

been compared using logic circuit and pulse of required width has been generated. To improve power quality of the system PD-PWM technique has been developed for the reduction in harmonic distortion.

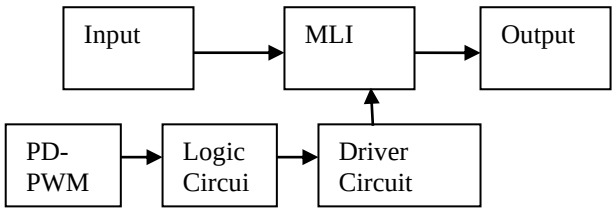


Fig. 11. Proposed basic block diagram

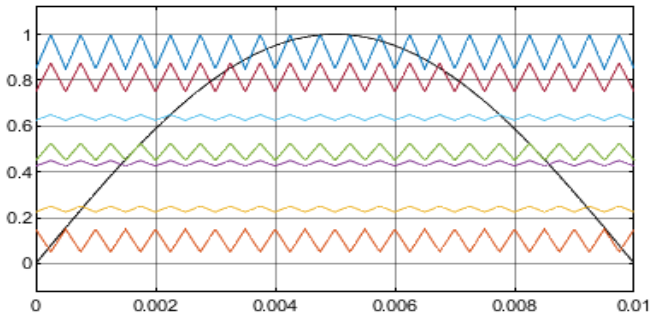


Fig. 12. Simulation result for PD-PWM pulse generation for 15 level reduced switch topology

For reduced switch topology number of carrier signal required

$$N = n$$

where, N = Number of carrier signals
n = Number of input dc source.

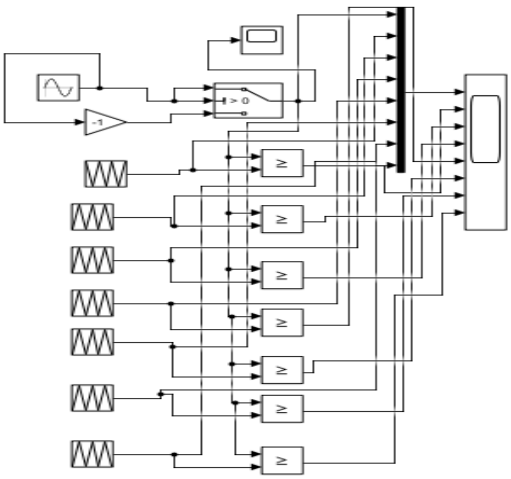


Fig.13. SIMULINK pulse generation circuit

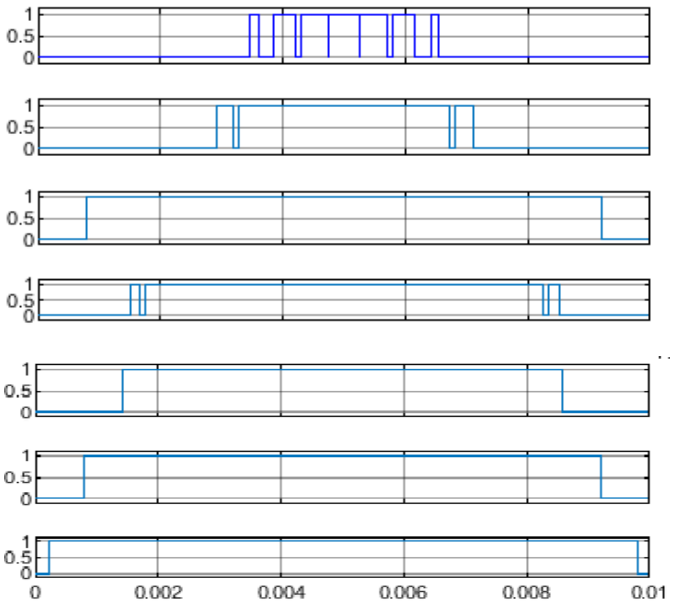


Fig. 14. Pulse generated for Sw1, Sw2, Sw3, Sw4, Sw5, Sw6 & Sw7 respectively

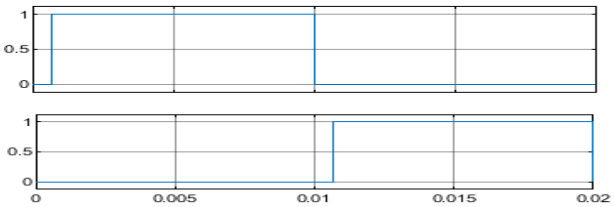


Fig. 15. Pulse generated for T1, T4 & T2, T3 respectively

The switching pulse of Sw1, Sw2, Sw3, Sw4, Sw5, Sw6 and Sw7 are shown in fig.14 and switching pulse of H-bridge inverter switches T1, T2, T3 and T4 are shown in fig. 15. The main advantage of this approach is that less distortion in the output voltage as a result can be applicable in high power quality applications**.**

VII. SIMULATION RESULTS AND DISCUSSION

Fig. 13. shows the PD-PWM circuit to generate gate pulses for MLI switches. In fig. 12. seven carrier signal and a reference signal is shown and compared. In fig. 14 by the comparison of reference and carrier signals pulses are generated for the reduced switch topology of 15 level inverter. THD analysis is done for both symmetrical as well as asymmetrical MLI. This proposed method has the ability to generate pulse to eliminate higher as well as lower order harmonics and this method has one more advantage is that because of half wave symmetry of output voltage the even harmonics get eliminated totally i.e. zero. In table II and III comparison is done for harmonics level.

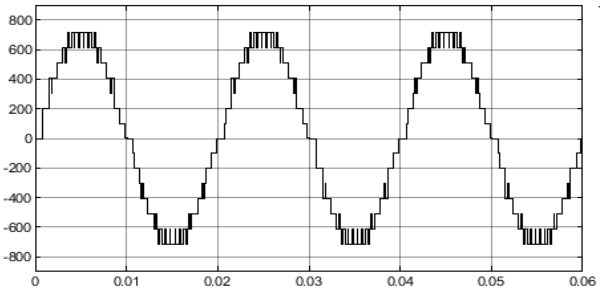


Fig. 16. 15 level output voltage waveform with PD-PWM

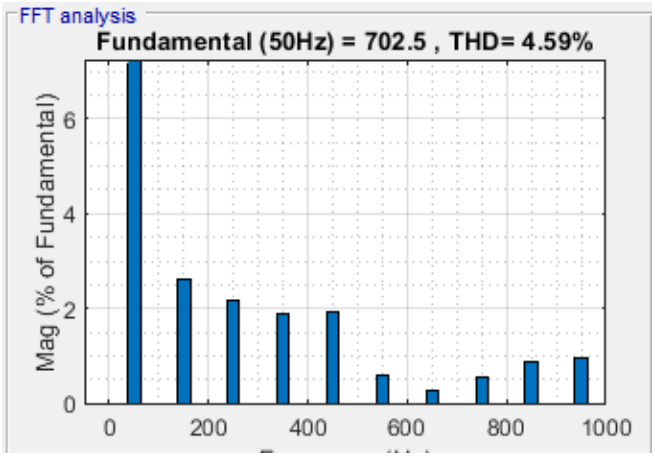
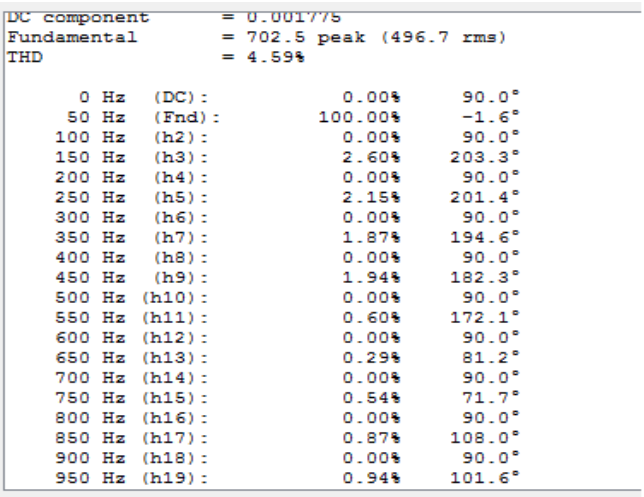


Fig. 17. FFT analysis for asymmetrical MLI with PD-PWM



```
DC component      = 0.001775
Fundamental       = 702.5 peak (496.7 rms)
THD               = 4.59%

   0 Hz   (DC):        0.00%     90.0°
  50 Hz   (Fnd):     100.00%     -1.6°
 100 Hz   (h2):        0.00%     90.0°
 150 Hz   (h3):        2.60%    203.3°
 200 Hz   (h4):        0.00%     90.0°
 250 Hz   (h5):        2.15%    201.4°
 300 Hz   (h6):        0.00%     90.0°
 350 Hz   (h7):        1.87%    194.6°
 400 Hz   (h8):        0.00%     90.0°
 450 Hz   (h9):        1.94%    182.3°
 500 Hz  (h10):        0.00%     90.0°
 550 Hz  (h11):        0.60%    172.1°
 600 Hz  (h12):        0.00%     90.0°
 650 Hz  (h13):        0.29%     81.2°
 700 Hz  (h14):        0.00%     90.0°
 750 Hz  (h15):        0.54%     71.7°
 800 Hz  (h16):        0.00%     90.0°
 850 Hz  (h17):        0.87%    108.0°
 900 Hz  (h18):        0.00%     90.0°
 950 Hz  (h19):        0.94%    101.6°
```

Fig. 18. FFT analysis in list view for asymmetrical MLI with PD-PWM

Asymmetrical voltage level are generated randomly from the normal distribution method. For symmetrical input voltage each dc source is of 100 volts and for asymmetrical input voltage the voltage levels are 104.0736v, 104.5290v, 100.6349v, 104.5669v, 103.1618v, 100.4877v & 101.3925volts respectively.

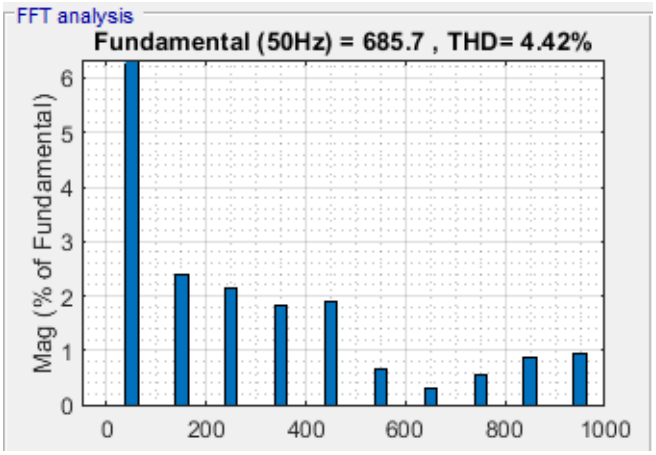


Fig. 19. FFT analysis for symmetrical MLI with PD-PWM

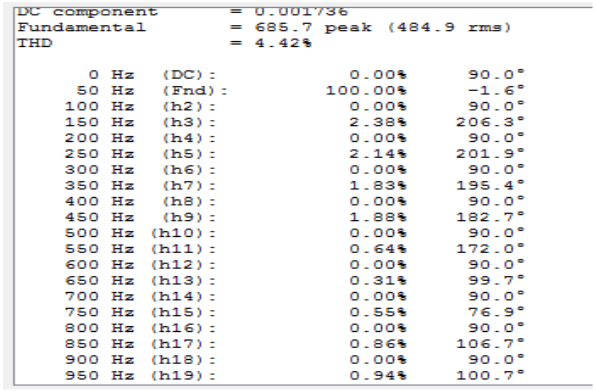


Fig. 20. FFT analysis in list view for symmetrical MLI with PD-PWM

Fig. 17 to 20 shows the THD profile from which we can clearly see that the harmonic level reduced. Reduced switch count and low level of THD both important factors are achieved . The overall system become more effective and with improved power quality profile.

Table- II: Symmetric MLI voltage harmonic comparison

Harmonic order	Measured value with switching states	Measured value with PD-PWM
1st	100	100
3rd	6.54	2.38
5th	5.24	2.14
11th	0.72	0.64
15th	0.68	0.55
19th	1.06	0.94
THD	**8.70%**	**4.42%**

Table-III: Asymmetric MLI voltage harmonic comparison

Harmonic order	Measured value with switching state	Measured value with PD-PWM
1st	100	100
3rd	6.85	2.60
5th	5.21	2.15
11th	0.79	0.60
15th	0.66	0.54
19th	1.08	0.94
THD	**8.94%**	**4.59%**

Table-IV: Comparison with other topology and method

Ref. No.	Level	No. of Switch	Methodology	THD %
[12]	11	11	PWM	9.07
[13]	15	18	SPWM	6.31
[12]	15	14	PWM	6.80
[14]	15	12	Fundamental-SHE	7.25
Proposed	**15**	**11**	**PD-PWM**	**4.42**

VIII. CONCLUSION

A PD-PWM based 15 level inverter is used with reduced switch count. The main focus of this paper is to improve the power quality for which some consideration has been achieved. Number of switch reduced, harmonics distortion has been reduced to 4.42%. Due to half wave symmetry of output voltage waveform the even order harmonics become zero. The results shows the effectiveness of proposed system. The THD get limited to 4.42% from 8.70% for symmetrical and 4.59% from 8.94% for asymmetrical topology by the application of PD-PWM technique and THD is under IEEE 519 standard i.e. <5%. A proper control method has been designed in order to make the system more efficient and to improve the power quality.

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AUTHORS PROFILE

Richa Gupta, Research scholar in Power Electronic, Electrical Engineering Department SGSITS, 23 park Road Indore (M. P.)India. She received her bachelor degree in Electrical and Electronics Engineering from University Institute of Technology, RGPV, Bhopal (M.P.) in 2017. Her research interest include power electronic, power quality, renewable energy analysis.