A Switched-Capacitor Inverter using Series/ Parallel Conversion with Inductive Load

M. Swarnalatha, G. devadas, K. sunil

Abstract - A novel switched-capacitor inverter is proposed. The proposed inverter outputs larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors. The proposed inverter, which does not need any inductors, can be smaller than a conventional two-stage unit which consists of a boost converter and an inverter bridge. Its output harmonics are reduced compared to a conventional voltage source single phase full bridge inverter. In this paper, the circuit configuration, the theoretical operation, the simulation results with MATLAB/ SIMULINK, and the experimental results are shown. The experimental results accorded with the theoretical calculation and the simulation results.

Index Terms—Charge pump, multicarrier PWM, multilevel inverter, switched capacitor (SC).

I. INTRODUCTION

Recently, electrical energy systems, electric vehicles (EVs), and dispersed generation (DG) systems, etc., are focused because of the global environmental issues. The power electronics, converters and inverters, is a key technology in these systems [1]–[6].

The EVs and the grid connected DG systems need an inverter to convert dc to ac. Boost converters or transformers are widely used in these systems when the input voltage is smaller than the output voltage. However, a transformer or an inductor in the boost converter makes the system large, because the transformer and the inductor must have large and heavy magnetic cores to sustain the high power [5]. As a provision against the issue, a charge pump, which does not have any inductors, is applied to such systems [7].

A charge pump outputs a larger voltage than the input voltage with switched capacitors [7], [8]. When the several capacitors and the input voltage sources are connected in parallel, the capacitors are charged. When the several capacitors and the input voltage sources are connected in series, the capacitors are discharged. The charge pump outputs the sum of the voltages of the capacitors and the input voltage sources. However, a charge pump has many switching devices which make the system more complicated. switched-capacitor (SC) inverter outputs multilevel voltages with switched capacitors [9], [10]. An SC inverter is similar to a charge pump in the topology. The SC inverter outputs a larger voltage than the input voltage in similar way to the charge pump. However, the SC inverter also has many switching devices which make the system complicated. On the other hand, a Marx inverter, which has less switching devices compared to the SC inverter, was proposed [11].

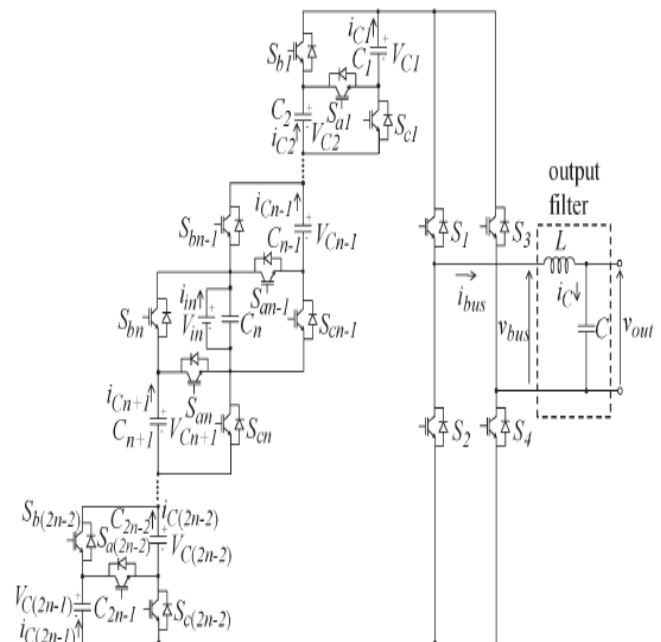Marx inverter can be regarded as one of the SC inverters because of its operation principle.

Fig. 1. Circuit topology of the switched-capacitor inverter using series/ parallel conversion.

In this paper, an SC inverter whose structure is simpler than the conventional SC inverter is proposed. It consists of a Marx inverter structure and an H-bridge. The proposed inverter can output larger voltage than the input voltage by switching the capacitors in series and in parallel. The proposed inverter does not have any inductors which make the system large. The output harmonics of the proposed inverter are reduced by the multilevel output.

In Section II, the circuit topology is introduced and the driving method is explained. In Section III, the determination method of the capacitance is described. In Section IV, losses in the proposed inverter are calculated and estimated. In Sections V and VI, simulation results with MATLAB/ SIMULINK and the results of the circuit experiments are shown.

II. CIRCUIT DESCRIPTION

Fig. 1 shows a circuit topology of the proposed inverter, where S_{ak}, S_{bk}, S_{ck} ($k = 1, 2, . . , 2n − 2$) are the switching devices which switch the capacitors C_k ($k = 1, 2, . . 2n − 1$) in series and in parallel. Switches $S_1 − S_4$ are in the inverter bridge. A voltage source V_{in} is the input voltage source. A low pass filter is composed of an inductor L and a capacitor C.

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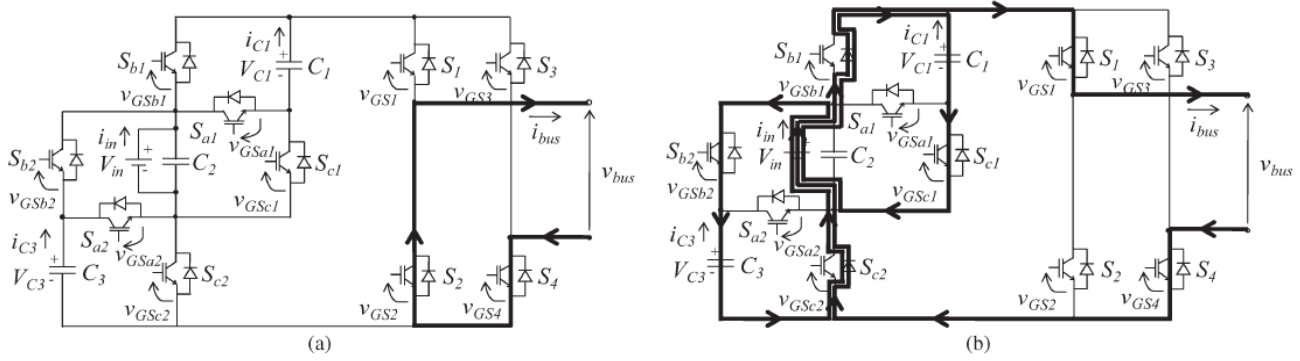

Fig. 2. Current flow of the proposed inverter ($n = 2$) on each state, (a) the current i_{bus} does not flow in the capacitors C_k, (b) all capacitors are connected in parallel, (c) the capacitor C_1 is connected in series and the capacitor C_3 is connected in parallel, and (d) all capacitors are connected in series.

There are many modulation methods to drive a multilevel inverter: the space vector modulation [3], [12]–[14], the multicarrier pulse width modulation (PWM) [3], [15], [16], the hybrid modulation [1], [3], [4], [17], the selective harmonic elimination [3], [18], [19], and the nearest level control [3]. In this paper, the multicarrier PWM method is applied to the proposed inverter.

Fig. 2 shows the current flow in the proposed inverter ($n = 2$) and Fig. 3 shows the modulation method of the proposed inverter ($n = 2$). When the time t satisfies $0 \leq t < t_1$ in Fig. 3, the switches S_1 and S_2 are driven by the gate-source voltage v_{GS1} and v_{GS2}, respectively. While the switches S_1 and S_2 are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in

Fig. 2(a) and (b) are switched alternately and the bus voltage v_{bus} takes 0 or V_{in}.

When the time t satisfies $t_1 \leq t < t_2$ in Fig. 3, the switches S_{a1}, S_{b1}, and S_{c1} are driven by the gate-source voltage v_{GSa1}, v_{GSb1}, and v_{GSc1}, respectively. While the switches S_{a1}, S_{b1}, and S_{c1} are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(b) and (c) are switched alternately. The capacitor C_1 is charged by the current $- i_{C1}$ as shown in Fig. 2(b) during the state shown in Fig. 2(b). Therefore, the proposed inverter can output the bus voltage v_{bus} while the capacitor C_1 is charged. The bus voltage v_{bus} in the state of Fig. 2(c) is

$$v_{bus} = V_{in} + V_{C1} \tag{1}$$

Where V_{C1} is the voltage of the capacitor C_1. Therefore, the proposed inverter outputs V_{in} or $V_{in} + V_{C1}$ alternately in this term.
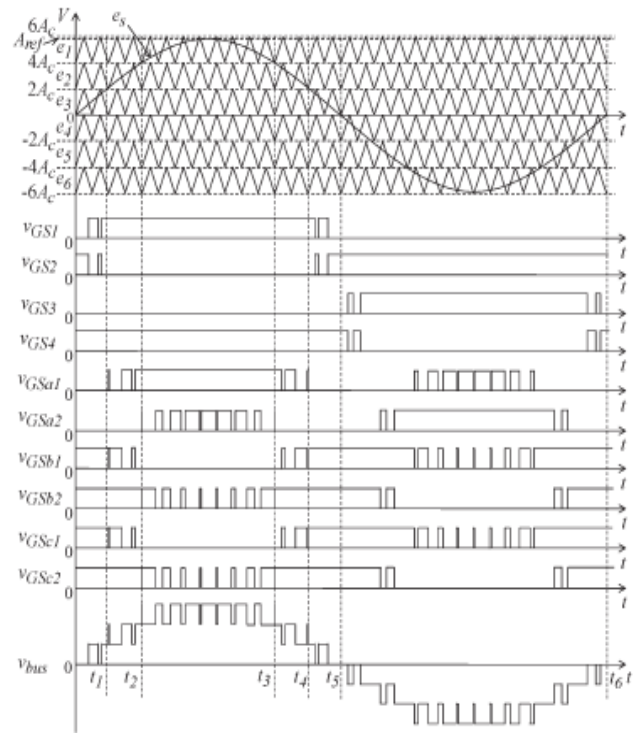

Fig. 3. Modulation method of the proposed inverter ($n = 2$).

When the time t satisfies $t_2 \leq t < t_3$ in Fig. 3, the switch S_{a2}, S_{b2} and S_{c2} are driven by the gate-source voltage v_{GSa2}, v_{GSb2} and v_{GSc2}, respectively. While the switches S_{a2}, S_{b2}, and S_{c2} are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(c) and (d) are switched alternately. The capacitor C_3 is charged by the current $- i_{C3}$ as shown in Fig. 2(c) during the state shown in Fig. 2(c). The bus voltage v_{bus} in the state of Fig. 2(d) is

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$$V_{bus} = V_{in} + V_{C1} + V_{C3} \qquad (2)$$

Where V_{C3} is the voltage of the capacitor C_3. Therefore, the proposed inverter outputs $V_{in} + V_{C1}$ or $V_{in} + V_{C1} + V_{C3}$ alternately in this term. After $t = t_3$, the four states shown in Fig. 2 are repeated by turns.

Table I shows the list of the on-state switches when the proposed inverter ($n = 2$) is driven by the modulation method shown in Fig. 3. The ideal bus voltage v_{bus} in Table I means the bus voltage on each state when $V_{C1} = V_{C3} = V_{in}$ is assumed. As the conventional SC inverter, the proposed inverter has a full bridge which is connected to the high voltage. Therefore, the device stress of the switches $S_1 - S_4$ in the full bridge is higher than the other switches as the conventional SC inverter.

TABLE I
LIST OF THE ON-STATE SWITCHES ON EACH STATE

Relation between e_s & e_k	On state switches	Ideal bus voltage V_{bus}
$e_s > e_1$	S_1, S_4, S_{a1}, S_{a2}	$3V_{in}$
$e_1 \geq e_s > e_2$	$S_1, S_4, S_{a1}, S_{b2}, S_{c2}$	$2V_{in}$
$e_2 \geq e_s > e_3$	$S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	V_{in}
$e_3 \geq e_s > e_4$	$S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	0
$e_4 \geq e_s > e_5$	$S_2, S_3, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$-V_{in}$
$e_5 \geq e_s > e_6$	$S_2, S_3, S_{b1}, S_{c1}, S_{a2}$	$2V_{in}$
$e_6 \geq e_s$	S_1, S_4, S_{a1}, S_{a2}	$-3V_{in}$

The proposed inverter ($n=2$) outputs a 7-level voltage by repeating the four states as shown in Fig. 2. Because the driving waveform v_{GSa1} and v_{GSa2} change alternately as shown in Fig. 3,the capacitors C_1 and C_3 are equally discharged. Assuming that the number of the capacitors is $2n-1$, the proposed inverter can outputs $4n-1$ levels voltage waveform.

The modulation index M is defined as the following equation because the amplitude of the output voltage waveform is inversely proportional to the double amplitude of the carrier waveform

$$M = A_{ref} / 2A_c \qquad . \quad (3)$$

In (3), A_{ref} is the amplitude of the reference waveform and A_c is the amplitude of the carrier waveform.

The proposed inverter requires 10 switching devices for the 7-level, and 16 switching devices for the 11-level. On the other hand, the conventional SC inverter requires 20 switching devices for the 7-level, and 28 switching devices for the 11-level [9]. The conventional cascaded H-bridge (CHB) inverter requires 12 switching devices for the 7-level, and 20 switching devices for the 11-level, when all the dc voltage sources take the same voltage [17]. Therefore, the proposed inverter has less number of switching devices than the conventional multilevel inverters.

III. DETERMINATION OF CAPACITANCE

The capacitance C_k can be determined properly with considering the voltage ripple of the capacitors C_k. The smaller voltage ripple of these capacitors leads to the higher efficiency. In this section, the capacitance C_k are calculated when the maximum voltage ripple is supposed to be 10% of the maximum voltages of the capacitors.

The capacitors C_k are charged when they are connected in parallel and are discharged when they are connected in series. From Fig. 3, the switches S_{a1} and S_{a2} of the proposed inverter ($n = 2$) are symmetrically driven during the half cycle of the reference waveform. Therefore, the voltage ripple of the capacitor C_1 is focused.

Assuming that the power factor of the output load $\cos \phi = 1$, the longest discharging term of the capacitor C_1 in the proposed inverter ($n = 2$) is between t_2 and t_3 in Fig. 3. Assuming the modulation index $M = 3$, the time t_1, t_2 and t_3 in Fig. 3 are

$$t_1 = \frac{\sin^{-1}(1/3)}{2\pi f_{ref}} \qquad (4)$$

$$t_2 = \frac{\sin^{-1}(2/3)}{2\pi f_{ref}} \qquad (5)$$

$$t_3 = \frac{\pi - \sin^{-1}(2/3)}{2\pi f_{ref}} \qquad (6)$$

where f_{ref} is the frequency of the reference waveform. Therefore, the maximum discharge amount Q_1 of the capacitor C_1 is

$$Q_1 = \int_{t_2}^{t_3} I_{bus} \sin(2\pi f_{ref}t - \phi)\, dt \qquad (7)$$

where I_{bus} is the amplitude of the bus current waveform and ϕ is the phase difference between the bus voltage waveform v_{bus} and the bus current waveform i_{bus}. Q_1 supposes to be less than 10% of the maximum charge of C_1. Therefore, the capacitance C_1 must satisfy

$$C_1 > \frac{Q_1}{0.1V_{in}}. \qquad (8)$$

When the capacitors C_k satisfy (8), the other voltage ripple which is caused by PWM is less than 10%. The peak current of the capacitor I_{C1} is calculated by

$$I_{C1} = \frac{V_{in} - V_{C1}}{r_{c1} + 2r_{on}} \qquad (9)$$

where r_{c1} is the equivalent series resistance (ESR) of the capacitor C_1 and r_{on} is the internal resistance of the switching devices. From (9), the peak current of the capacitor C_1 is determined by the difference between the input voltage V_{in} and the voltage of the capacitor V_{C1}, and the internal resistance of the switching devices. The difference of the voltages $V_{in} - V_{C1}$ is small when the capacitance C_1 is large. Therefore, when the switches which have small internal resistance are used the capacitance C_1 must be larger to prevent the large peak current.

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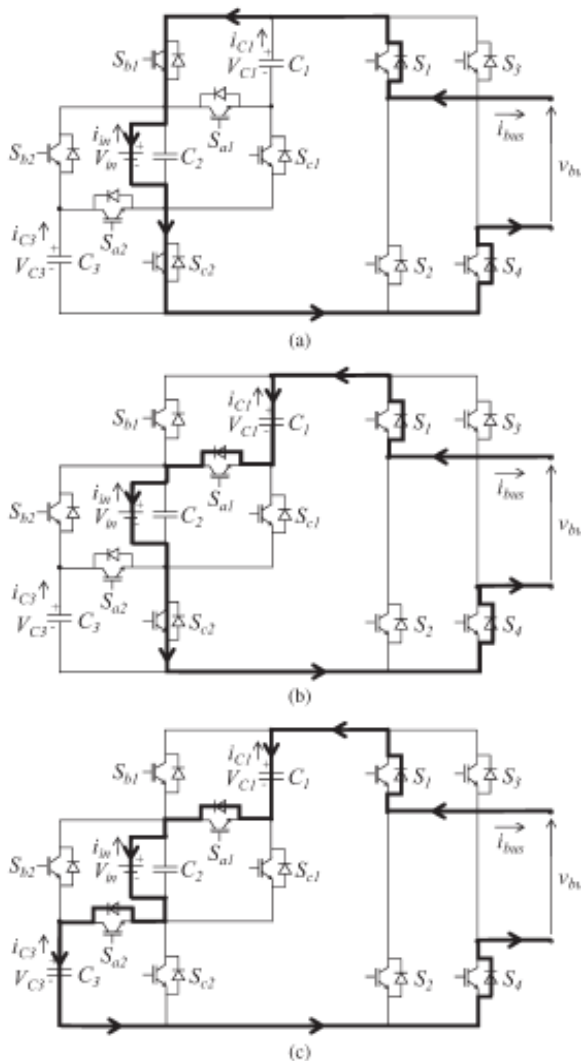

Fig. 4. Current flow of the proposed inverter ($n = 2$) with an inductive load, (a) all capacitors are connected in parallel, (b) the capacitor C_1 is connected in series and the capacitor C_3 is connected in parallel, and (c) all capacitors are connected in series.

, When the phase difference ϕ satisfies $0 < \phi < \sin^{-1}(2/3)$ i.e., $0.745 < \cos \phi < 1$, the current flows as shown in Fig. 4(a) and (b) before $t = \phi / 2 \pi f_{ref}$. Therefore, the capacitor C_1 is charged by the reverse current and the voltage of the capacitor C_1 is increased in the state when C_1 is connected in series as shown in Fig. 4(b). The charge amount Q_1 of the capacitor C_1 in the state is calculated by

$$Q_1' = - \int_{t_1}^{t_2} D_{Sa1}(t) I_{bus} \sin(2\pi f_{ref}t - \phi)\, dt \tag{10}$$

where $D_{Sa1}(t)$ is the duty ratio of the switch S_{a1}. From Fig. 3, $D_{Sa1}(t)$ is sinusoidal function between t_1 and t_2. In addition, $D_{Sa1}(t_1) = 0$ and $D_{Sa1}(t_2) = 1$. Therefore, $D_{Sa1}(t)$ is calculated by

$$D_{Sa1}(t) = 3\sin(2\pi f_{ref}t) - 1. \tag{11}$$

From (7) and (10), the maximum discharge amount Q_1 is larger than the charge amount $Q_{l\,1}$. Therefore, the voltage ripple of the capacitor C_1 is determined by Q_1 when $0.745 < \cos \phi < 1$.

When the power factor $\cos \phi$ satisfies $\cos \phi \leq 0.745$, there is the term when the current direction becomes reverse in all

states of the switching devices as shown in Fig. 4. Therefore, the maximum discharge amount Q_1 is calculated by

$$Q_1 = \int_{\frac{\phi}{2\pi f_{ref}}}^{t_2} I_{bus} \sin(2\pi f_{ref}t - \phi)\, dt. \tag{12}$$

From (7) and (12), the maximum discharge amount Q_1 is reduced. However, Q_1 is larger than the charge amount Q_1 because the input current is larger than the reverse current with an inductive load. Therefore, voltage ripple of the capacitor C_1 is also determined by Q_1 when the power factor $\cos \phi \leq 0.745$. The maximum discharge amount Q_1 takes the largest value when $\cos \phi = 1$ because the peak current is accorded to the peak voltage. Hence, when the capacitance C_k is determined for $\cos \phi = 1$, the proposed inverter can maintain the output waveform for $\cos \phi < 1$.

IV. CALCULATION OF LOSSES

In this section, the power losses of the proposed inverter ($n=2$) are calculated. In the calculation, the following losses are considered:
• switching losses;
• conduction losses of the switches;
• conduction loss of the output filter;
• conduction losses and losses caused by the voltage ripple of the capacitors C_k.

These losses are calculated about the proposed inverter ($n = 2$).

A. Switching Losses
In this section, switching losses are calculated from the charge and the discharge of the parasitic capacitance [20]. From Fig. 3, the switches S_1 and S_2 are switched ON/OFF at the carrier frequency f when the reference waveform e_s satisfies

$$|e_s| < \frac{1}{M}A_{ref}. \tag{13}$$

Therefore, the switches S_1 and S_2 are switched ON/OFF when the time t satisfies $0 < t < t_1$ or $t_4 < t < t_5$ in Fig. 3. When the reference waveform e_s does not satisfy (13), the switches S_1 and S_2 are maintained ON or OFF. Therefore, when the carrier waveforms and the reference waveform are not synchronous waveforms, the average number of switching transitions N_{S1} and N_{S2} in one period of reference waveform is calculated as

$$\overline{N_{S1}} = \overline{N_{S2}} = \frac{t_1 + (t_5 - t_4)}{t_6} \cdot \frac{2f}{f_{ref}}$$
$$= \frac{2\sin^{-1}(1/M)}{2\pi} \cdot \frac{2f}{f_{ref}} \tag{14}$$

where f is the switching frequency. When the carrier waveforms and the reference waveform are synchronous waveforms, the number of switching transitions is the maximum even number less than N_{S1} or $N_{S1} + 4$. The number of switching transitions is variable depending on the frequency modulation ratio f/f_{ref}. Therefore, when the synchronous waveforms are used in this modulation, the individual analysis is needed in each frequency modulation ratio.

In this paper, the switching losses are calculated with the average number of switching transitions N_{Sk}, because the high switching frequency f is assumed. For one second, this switching terms repeat f_{ref} times. Therefore, the switches S_1 and S_2 are switched $N_{S1} f_{ref}$ times and $N_{S2} f_{ref}$ times in one second, respectively. The same argument can be applied to the switches S_3 and S_4. The energy loss E_{loss} as the following equation occurs in one switching [20]

$$E_{loss} = \frac{1}{2} C_s V_{in}^2 \qquad (15)$$

where C_s is the parasitic capacitance of the switching devices. Therefore, the switching losses of these switches $P_{Sk}(k = 1, 2, 3, 4)$ are given as

$$P_{Sk} = \frac{2 \sin^{-1}(1/M)}{2\pi} \cdot C_s V_{in}^2 f. \qquad (16)$$

The switches S_{ak}, S_{bk}, and S_{ck} ($k = 1, 2$) are operated alternately in each cycle of the reference waveform. Therefore, the switching losses of these switches can be calculated with considering the half cycle of the reference waveform. If the voltage ripple of the capacitors C_k is ignored, i.e., the voltage of the capacitors $V_{Ck} = V_{in}$ is assumed, the switching losses of the switches S_{ak}, S_{bk}, and $S_{ck}(k = 1, 2)$ are calculated as the following equations by the same calculation method to the (16)

$$P_{Sa1} = P_{Sb1} = P_{Sc1}$$
$$= \frac{2\left\{\sin^{-1}(2/M) - \sin^{-1}(1/M)\right\}}{\pi} \cdot C_s V_{in}^2 f \qquad (17)$$

$$P_{Sa2} = P_{Sb2} = P_{Sc2} = \frac{\pi - 2\sin^{-1}(2/M)}{\pi} \cdot C_s V_{in}^2 f. \qquad (18)$$

All switching devices are switched when the voltage of each device is V_{in}. Therefore, the switching losses of the proposed inverter are smaller than the conventional voltage source full bridge inverter.

B. Conduction Losses of the Switches

There are three states on the proposed inverter ($n = 2$) as shown in Fig. 2; the state when all capacitors are connected in parallel, the state when one of the capacitors is connected in series, and the state when all capacitors are connected in series. However, it is obvious that the bus current i_{bus} flows in 4 switches on each state from Fig. 2. Therefore, the total conduction loss P_{sr} of the switches is calculated by

$$P_{sr} = 4 \cdot \frac{2\pi f_{ref}}{\pi} \int_0^{\frac{\pi}{2\pi f_{ref}}} r_{on} i_{bus}^2 \, dt \qquad (19)$$

where r_{on} is the internal resistance of the switching devices. On the other hand, the current flows in 6 switches in the conventional 7-level CHB inverter because the current flows in 2 switches in each H-bridge. Therefore, the total conduction loss of the switches in the conventional 7-level CHB inverter P_{CHB} is calculated as

$$P_{CHB} = 6 \cdot \frac{2\pi f_{ref}}{\pi} \int_0^{\frac{\pi}{2\pi f_{ref}}} r_{on} i_{bus}^2 \, dt. \qquad (20)$$

From (19) and (20), it is obvious that the conduction losses of the proposed inverter are less than the conventional 7-level CHB inverter when the same switching devices are used.

C. Conduction Loss of the Output Filter

The conduction losses of the filter inductance P_l and the filter capacitance P_c are calculated as the following equations:

$$P_l = r_l i_{bus}^2 \qquad (21)$$

$$P_c = r_c i_c^2. \qquad (22)$$

In (21), r_l is the ESR of the filter inductance L. In (22), r_c and i_c are the ESR and the current of the filter capacitance C.

D. Losses of the Capacitors C_k

When the capacitors $C_k(k \leq 2)$ are connected in parallel, the losses occur by the difference between the input voltage V_{in} and the voltages of the capacitors V_{Ck}. The voltage ripple of the capacitors ΔV_k is calculated by

$$\Delta V_k = \frac{1}{C_k} \int_{t_2}^{t_3} i_{Ck} \, dt \qquad (23)$$

where i_{Ck} is the current of the capacitor C_k and t_2, t_3 are the time when the capacitors C_k are connected in series as shown in Fig. 3. Therefore, the losses P_{rip} by this voltage ripple are calculated as the following equation.

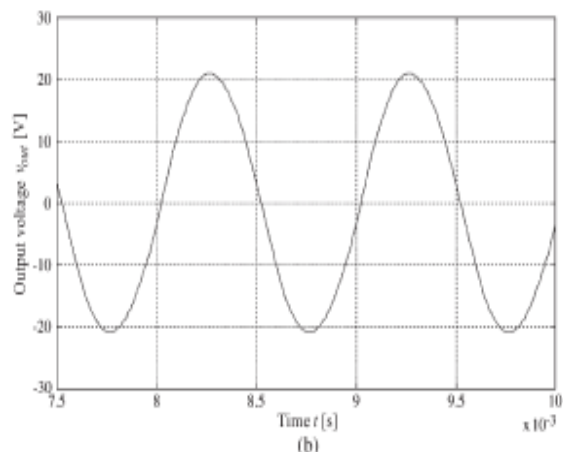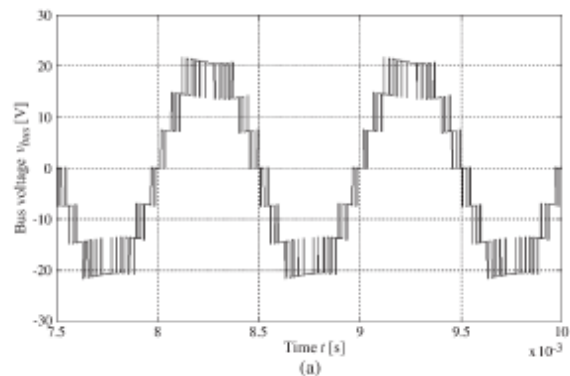$$P_{rip} = \sum_{k=1}^{2n-1} C_k \Delta V_k^2 f_{ref}. \qquad (24)$$

Fig. 5. Simulated voltage waveforms of the proposed inverter (n = 2) designed for low power at 5.76 [W], switching frequency f = 40 [kHz] and reference waveform frequency f_{ref} = 1 [kHz]. (a) Bus voltage waveform V_{bus} and (b) the output voltage waveform V_{out}.

From (23) and (24), the loss P_{rip} is inversely proportional to the capacitance C_k, which means the larger capacitance leads to the higher efficiency. When the capacitors C_k are connected in series, the lossesm occur by the internal resistance r_{sc}. The conduction losses of these capacitors P_{sc} are calculated by the following equation:

$$P_{sc} = \frac{2\pi f_{ref}}{\pi} \sum_{k=1}^{2n-1} \int_{\frac{\sin^{-1}(2/3)}{2\pi f_{ref}}}^{\frac{\pi - \sin^{-1}(2/3)}{2\pi f_{ref}}} r_{sc} i_{Ck}^2 \, dt. \quad (25)$$

V. SIMULATION RESULTS

Simulation was performed under the two conditions. One was for a low power inverter under the same condition with the circuit experiments. The other one was for a high power inverter.

The low power inverter simulation was performed with MATLAB/SIMULINK ver. R2009a under the following conditions. The MOSFET models whose internal resistance $R_{on} = 0.54$ [Ω] and the snubber resistance $R_s = 10_5$ [Ω] were used as the switching devices. The input voltage $V_{in} = 8.00$ [V], the output resistance $R = 50.0$ [Ω], a filter capacitance C, and a filter inductance L were $C = 0.450$ [μF] and $L = 1.13$ [mH], the modulation index $M = 3.00$, the switching frequency $f = 40.0$ [kHz], and the reference waveform frequency $f_{ref} = 1.00$ [kHz]. From (8), the capacitance C_1 and C_3 are calculated to $C_1 = C_3 = 143$ [μF], which have ESRs $r_{c1} = r_{c3} = 800$ [mΩ].

Fig. 5 shows the simulated voltage waveforms of the proposed inverter ($n = 2$) designed for low power at 5.76 [W].

The voltages of the capacitors V_{Ck} are changed between6.73 [V] and 7.51 [V]. Therefore, the voltage of the step in the bus voltage waveform decreases to about 90% as shown at $t = 8.11$ - to 8.40 [ms] in Fig. 5(a). It is caused by the 10% voltage drop at the capacitors C_k. This is accorded with the theoretical calculation. The theoretical amplitude of the output waveform is

$$MV_{in} = 24 \text{ [V]} \quad . \quad (26)$$

From Fig. 5(b) and (26), it is confirmed that the amplitude of the output waveform in the simulation is smaller than the theoretical amplitude. It is also caused by the voltage reduction of the capacitors C_k.

The high power inverter simulation was performed under the following conditions. The IGBT/Diode models whose internal resistance $R_{on} = 65.0$ [mΩ] and the snubber resistance $R_s = 10_5$ [Ω] were used as the switching devices. $V_{in} = 100$ [V], $R = 10.0$ [Ω], $C = 2.25$ [μF], $L = 225$ [μH], $M = 3.00$, $f = 40.0$ [kHz] and $f_{ref} = 1.00$ [kHz]. From (8), C_1 and C_3 are calculated to $C_1 = C_3 = 712$ [μF]. These capacitors ESRs r_{c1} and r_{c3} are 100 [mΩ].

Fig. 6 shows the simulated voltage waveforms of the proposed inverter ($n = 2$) designed for high power at 4.50 [kW]. The voltages of the capacitors V_{Ck} are changed between 87.0 [V] and 97.2 [V]. Therefore, the voltage of the step in the bus voltage waveform decreases to about 90% as shown at $t = 8.11$ - to 8.40 [ms] in Fig. 6(a), which is the same to the simulation result in low power models. The theoretical amplitude of the output waveform is

$$MV_{in} = 300 \text{ [V]}. \quad (27)$$

From Fig. 6(b) and (27), it is confirmed that the amplitude of

the output waveform in the simulation is smaller than the theoretical amplitude. As the result of the simulation in low power models, the voltage reduction of the capacitors C_k appears on the bus voltage waveform.

Fig. 7 shows the simulated current waveforms of the capacitor C_1 in the proposed inverter ($n = 2$). From the (9) and the voltage of the capacitor C_1, the absolute value of the peak current of the capacitor C_1 under the conditions of the low power and the high power simulations are 0.676 [A] and 56.5 [A], respectively. On the other hand, the absolute values of the peak currents in the simulation results are 0.605 [A] and 52.3 [A], respectively. The differences between the theoretical currents and the simulation results are caused by the nonlinear characteristic of the switching device models in MATLAB/SIMULINK.

Fig. 8 shows the simulated spectra of the bus voltage waveform, which are normalized with the fundamental component.
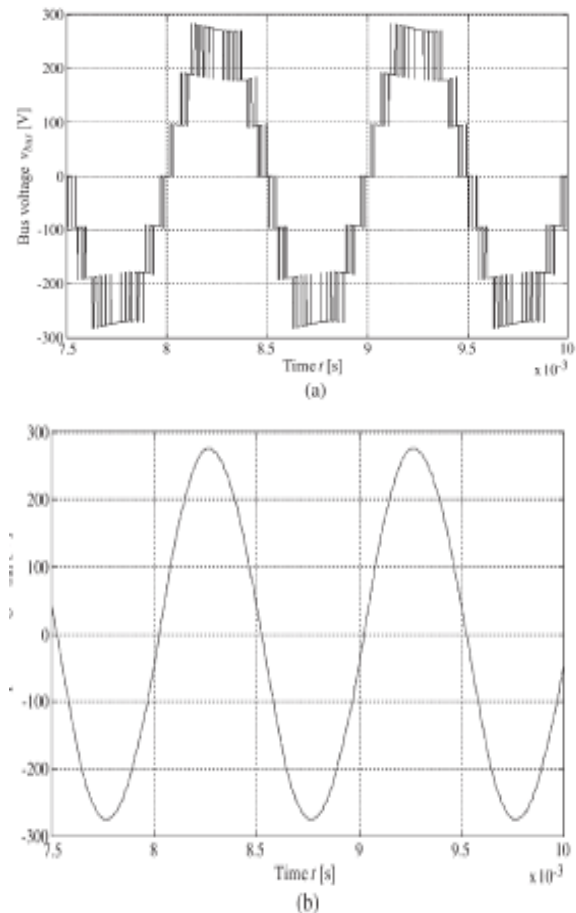

Fig. 6. Simulated voltage waveforms of the proposed inverter (n = 2) designed for high power at 4.50 [kW], switching frequency f = 40 [kHz] and reference waveform frequency f_{ref} = 1 [kHz]. (a) Bus voltage waveform v_{bus} and (b) the output voltage waveform v_{out}.
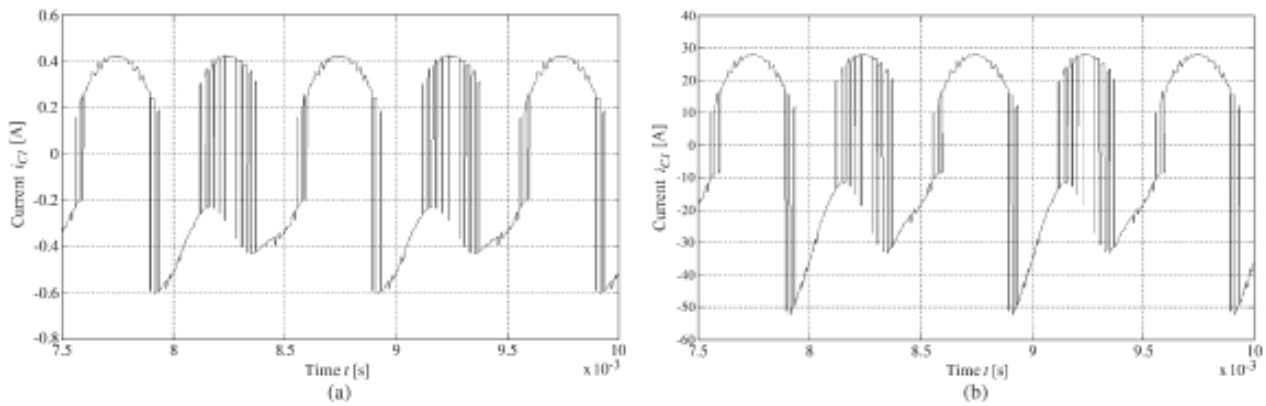
Fig. 7. Simulated current waveforms of the capacitor i_{C1} in the proposed inverter (n = 2).(a) Designed for low power at 5.76 [W] and (b) designed for high power at 4.50 [kW].
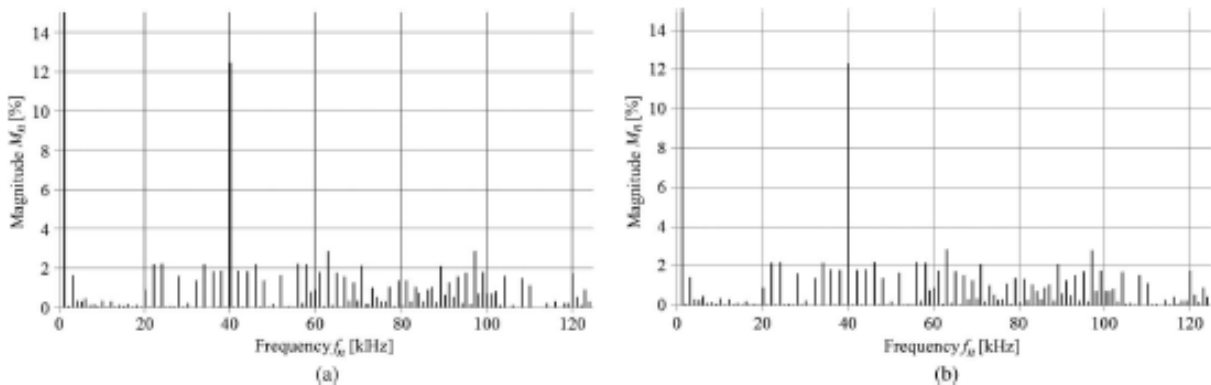

Fig. 8. Simulated spectra of the bus voltage waveform of the proposed inverters (n = 2) normalized with the fundamental component. (a) Designed for low power at 5.76 [W] and (b) designed for high power at 4.50 [kW].

In both spectra of the bus voltage waveforms of the low power and the high power proposed inverters, the magnitude at 40 [kHz] is larger than the other frequency components. This is caused by the switching frequency f = 40 [kHz]. The calculated total harmonic distortions (THDs) of the 5.76 [W] inverter and of the 4.50 [kW] inverter are 18.9% and 18.7%. On the other hand, the THD of the conventional voltage source single phase full bridge inverter is 64.3% under the same condition of the low power simulation. The THDs of the proposed inverters are reduced compared to the conventional single phase full bridge inverter.
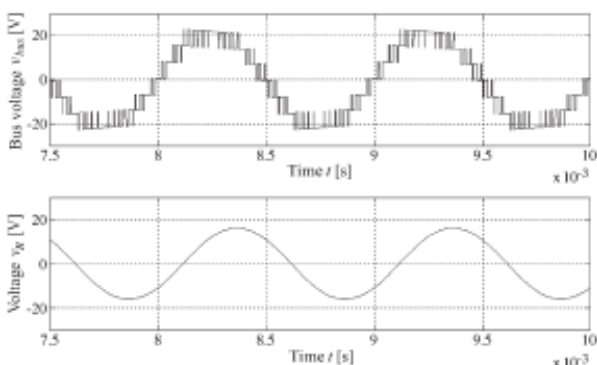

Fig. 9 shows the simulated output voltage waveforms with an inductive load under the same condition of the low power inverter simulation. The load inductance $L_R = 4.89$ [mH] and the load resistance $R = 40.0$ [Ω] are connected in series as the inductive load. The power factor of the inductive load

VII. CONCLUSION

In this paper, a novel boost switched-capacitor inverter was proposed. The circuit topology was introduced. The modulation method, the determination method of the capacitance, and the loss calculation of the proposed inverter were shown. The circuit operation of the proposed inverter was confirmed by the simulation results and the experimental results with a resistive load and an inductive load.

The proposed inverter outputs a larger voltage than the input voltage by switching the capacitors in series and in parallel. The inverter can operate with an inductive load. The structure of the inverter is simpler than the conventional switched-capacitor inverters. THD of the output waveform of the inverter is reduced compared to the conventional single phase full bridge inverter as the conventional multilevel inverter.

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