Power Efficient Double Gate MOSFET Full Adder Circuit using 45nm Technology

Rajesh Kumar Panda, Ralesh Ranjan Biswal, Jyoti Sankar Sahoo

Abstract*-- In designing an arithmetic circuit many aspects are to be taken into consideration. The main aspect is the power consumption. It is a tough task for the designers to design a circuit which consume less power in standby mode as well as in active mode. In an arithmetic circuit, the adder is an important module not only for addition operation but it is also the nucleus for many arithmetic operations. Hence it is required to reduce the power consumption of adder circuit in order to reduce the power consumption of the arithmetic module. As the efficiency of adder circuit is directly influence the efficiency of the arithmetic circuit, therefore many designs have been proposed in various literatures to resolve this issue. The very promising and advanced design is to implement the full adder circuit with double gate MOSFET. As technology growing, the full adder is now implemented by using 10 number of double gate transistors instead of 28 transistors as in the peer CMOS design. But still the power consumption of this circuit is not appreciably reduced. In this paper we proposed a design which is made up of 10T double gate (DG) MOSFETs in which all the bodies of P-type Double Gate-MOSFETs are connected to a supply less than the main supply and all the bodies of N-type Double Gate-MOSFETs are connected to another supply voltage whose value is slightly greater than zero. In the earlier design the output is not prominently stated but in this proposed modified design the output waveform is clearly distinguished by adding extra buffers to the output. In this new proposed design the static or standby power is reduced nearby 93% and the total power is reduced nearby 79% as compared to the earlier design. Simulation results of the proposed modified design is performed by cadence virtuoso with 45nm technology for validation.

Index Terms- DG-MOSFET, 10T Full adder, Low power adder circuit

I. INTRODUCTION

An arithmetic circuit has many design parameters. Among those parameters adder is an important parameter to determine the efficiency of the arithmetic circuit. Hence enhancing its performance is the crucial factor for enhancing the overall module performance [1, 2]. So it's a big challenge for the designer to design an adder circuit considering leakage current, active power and delay. These parameters are directly affecting the performance of the arithmetic circuit. Many adder designs have been proposed which generally focused on leakage power reduction, delay reduction etc. A conventional adder circuit is made up of 28 transistors which requires a large area and also consumes a large amount of leakage power [3]. Hence designs using 10T double gate transistor adder circuit[4] have been proposed with less number of transistors in order to reduce the area as well as leakage power. These designs suffered from a high leakage power and the outputs were not prominent. Hence we proposed a modified design of 10T double gate transistors adder circuit. In this proposed design we have sacrificed the area but it has the prime advantage of very less leakage power as compare to its peer design. The use of double gate MOSFET is quite obvious because it has the advantages such as its control over short channel effect, reduced power consumption, area etc [5]. As per the name double gate has two gates which helps for a flexible design in low power applications [6]. It has better electrostatic control over channel charges which makes it an important device for reduction of short-channel effects [7].

The rest of the paper is organised in the following ways. Double gate MOSFET and its advantages over single gate MOSFET including its related works is described in Section 2. The Section 3 presents the proposed modified 10T full adder circuit. Section 4 deals with the complete simulation results of the proposed model. The conclusion of the paper is presented in Section 5.

II. DOUBLE GATE MOSFET: STRUCTURE, ADVANTAGES AND RELATED WORK

A.Conventional DG-MOSFET Structure

Double Gate MOSFET structure is emerging as the most prominent technology for low power circuit designs. The key theme of a double-gate MOSFET (DGFET) is to have a channel of scaled width and to manage that channel, gate contacts are given to both the sides [8]. The two types of gates namely the Front gate and Back gate in DG-MOSFET can independently driven to reduce the power consumption and improve the performance of the device [9]. Double-Gate MOSFET (DG) devices are otherwise known as scalable silicon transistors because of its tremendous control of the short-channel effects in the double-gate structure [10, 11]. There are four different kinds of DG-MOSFET designs are available such as the **tied** symmetric and asymmetric double gates, and the **separated** symmetric and asymmetric double gates [12] as shown in Fig. 1. In the tied structure, the two gates are supplied with same potential and on the contrary in the separated structure, both gates are supplied with different potentials.

Manuscript Received May 5, 2015.

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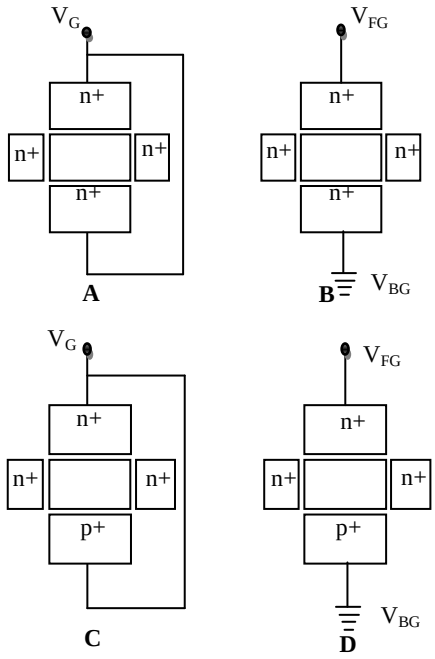

Figure 1. Schematics of various types of DG-MOSFETs (A) Symmetric Tied DG-MOSFET, (B) Symmetric Independent DG-MOSFET, (C) Asymmetric Tied DG-MOSFET, (D) Asymmetric Independent DG-MOSFET [8].

While both gates are independent, the front gate is the functional gate and the back gate is used as the secondary gate to adjust threshold voltage [12]. In a DG-MOSFET when two gates are coupled with each other then it can reduce the short channel effects and leakage. The double gate transistors are operated with very small input voltage in comparison to the existing CMOS transistors which in terms indicate reduced power consumption [4]. As in DG-MOSFET the short channel effect is controlled by both the gates so heavy doping is not necessary [13].

B. Advantages of DG-MOSFET

Double gate structure increase the efficiency of transistors as compare to the planer CMOS transistors. The efficiency of DG-MOSFET increases because its scaled Si channel width as compare to the single gate transistor. Here in this design the gate to channel coupling is doubled so that the short channel effect is easily suppressed. In DG-MOSFET device very low doped or un-doped channel is formed which gives good carrier mobility as compared to the planer CMOS transistors and gives better intrinsic switching time and reduced leakage current. The gate terminals are supplied with the voltage which direct the current conduction through the channel [14].

C. Full Adder

Full adder is a combinational circuit which perform addition of the supplied inputs. The Full adder (as shown in Fig. 2) is the circuit that takes three numbers of inputs and give two outputs i.e. sum and carry. The inputs are generally given as *a*, *b*, C_{in}. The full adder can be designed with XOR gates and one inverter. It can add binary numbers of 8, 16, 32 bits etc. The circuit generates two outputs, namely output carry(C_{out}) and sum(*Sum*) as given in equations (1), (2) and (3).

$$Sum = 2 * C_{out} + S \quad (1)$$

$$Sum = a \oplus b \oplus C_{in} \quad (2)$$

$$C_{out} = a \times b + b \times C_{in} + C_{in} \times a \quad (3)$$

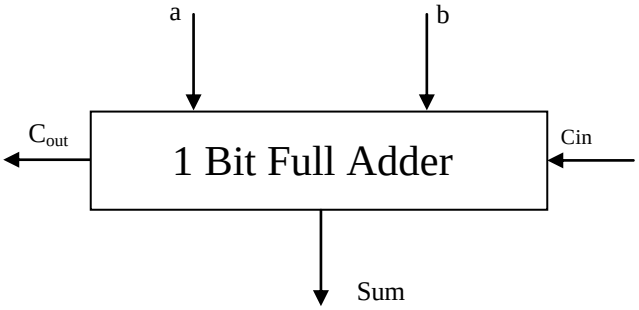

Figure 2. Full Adder block diagram (1 bit)

D. Related work on Full adder using DG-MOSFET

The previously proposed 10T full adder circuit design using DG-MOSFET has many advantages like less area, high speed, less delay and power as compared to the full adder circuit based on CMOS. The 10T full adder using DG-MOSFET model was implemented by using two 4T XOR gate followed by an inverter circuit. The XOR is the fundamental building block of a full adder circuit and the main function that is the addition is done by it. So this model of full adder was constructed by XOR circuit with less number of transistors i.e. 4 number to reduce the power consumption and improve the speed [15, 16]. Reduction in the size of full adder was achieved by implementing the 4T XOR gate in that circuit. The model is shown in Fig. 3 and the output is shown in Fig. 4 and the power waveform is shown in Fig. 5.

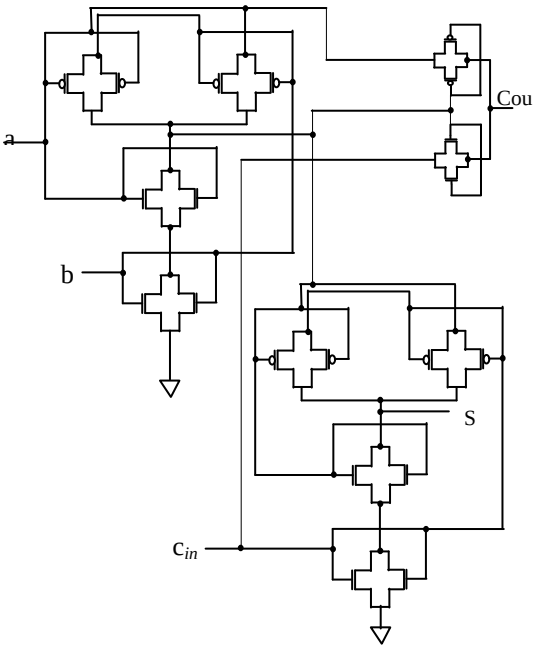

Figure 3. 10T Full Adder using Double Gate MOSFET

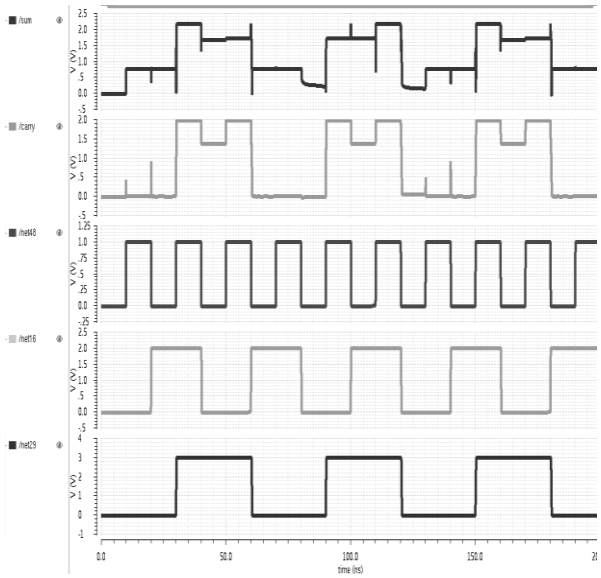

Figure 4. Output waveform of 10T full adder circuit using DG-MOSFET

In the above 10T full adder design by DG-MOSFET the output was not prominent and suffered by high voltage swing. Due to this voltage swing the output produced by the eight input sets are not clearly defined. And due to this the dynamic power consumption of the total circuit will increased.

E. Disadvantages of the above full adder circuit

The concerned circuit suffered with various problems like glitch [3] in the output waveform, power consumption etc. The power consumption is reduced to a significant mark in the proposed modified design. One method to reduce the glitch is to add buffer gates at the respective inputs which reduces the glitch in the output to an appreciable mark. In this design all the bodies of P-type DG-MOSFETs and N-type DG-MOSFETs are connected to the power supply and to the ground respectively thus the leakage current flow exceeds its tolerable limits. And also by this connection of bodies with the supply or ground the power consumption by the circuit was increased. These unavoidable disadvantages are tried to overcome in the proposed modified design. The power plot and the calculated power are given below. The modified design with its advantages is presented in Section 4.

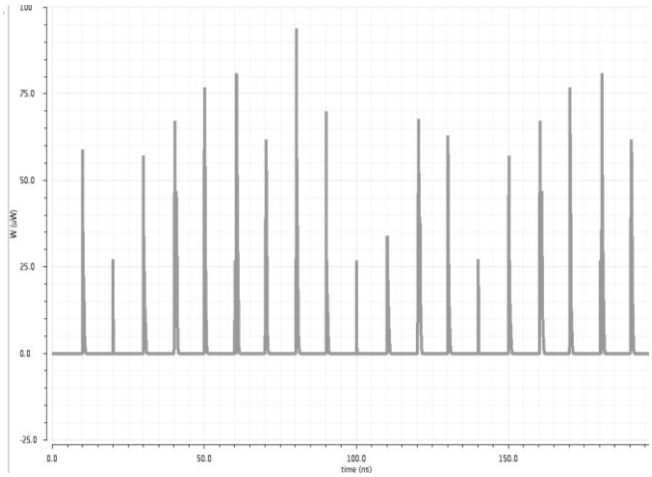

Figure 5. Power waveform of 10T Full Adder using DG-MOSFET

III. PROPOSED MODIFIED DESIGN FOR 10T FULL ADDER

As the previous design suffered with a significant amount of power consumption as well as the output was not so prominent hence a newly modified and improved design is proposed in this paper. The design proposed here consumes very less power as compare to the previous design but by sacrificing the area. All the bodies of the p-type DG-MOSFETs are connected to a supply having voltage less than the main supply voltage. And all the bodies of n-type DG-MOSFETs are connected to a supply having voltage slightly greater than the ground voltage. In this way the extra power consumption by the bodies is reduced appreciably as compared to the circuit where the bodies are directly connected to the main supply voltage. In the previous design the output was not prominent as per the Fig. 4. In this proposed modified design the output is connected to a buffer for introducing a delay. After inserting a delay element the output is clearly visible. Another modification with this device is that the W/L ratio is kept at 3. That means the sizing of the device is done in consideration of W/L ratio. The proposed design is implemented by using two 4T XOR gates and an inverter. The proposed design, its output waveform and power waveform are shown in Fig. 6, Fig. 7 and Fig. 8 respectively. The design is done with Cadence Virtuoso 45nm technology with room temperature of 27^oC.

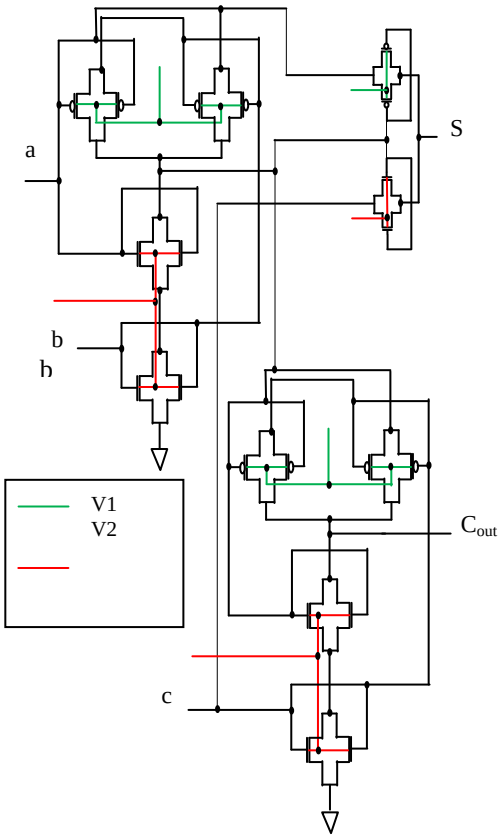

Figure 6. Full adder using double gate MOSFET

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In the proposed design the output is more prominent and the states are well distinct. The corresponding output waveform is shown in Fig. 7.

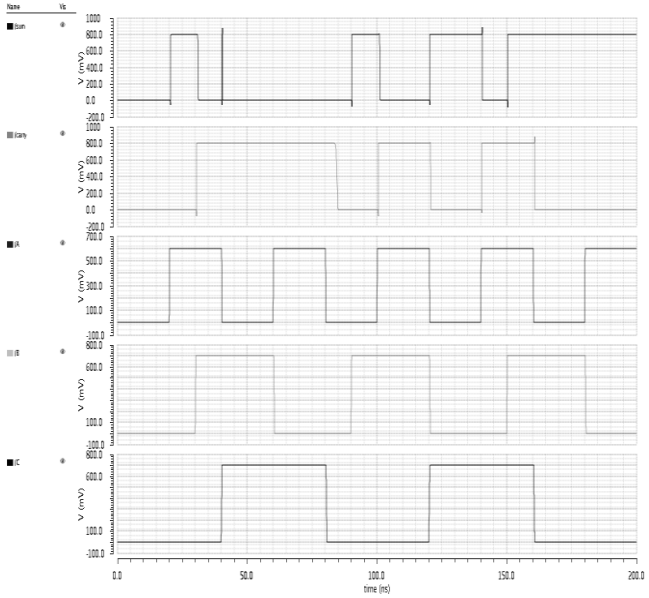


Figure 7. Output waveform of the proposed 10T full adder circuit.

IV. SIMULATION AND RESULTS

The previously proposed one bit 10T full adder circuit using double gate MOSFET is modified in this paper. Simulation of the newly proposed design is completed by using Cadence Virtuoso 45nm tool at $27^{o}C$ room temperature.

From the design, the average power can be calculated as follows,

$$P_{avg} = P_{static} + P_{dynamic} \quad (4)$$

The static power is calculated by doing DC analysis of the circuits. The static power plot is shown in Fig. 8.

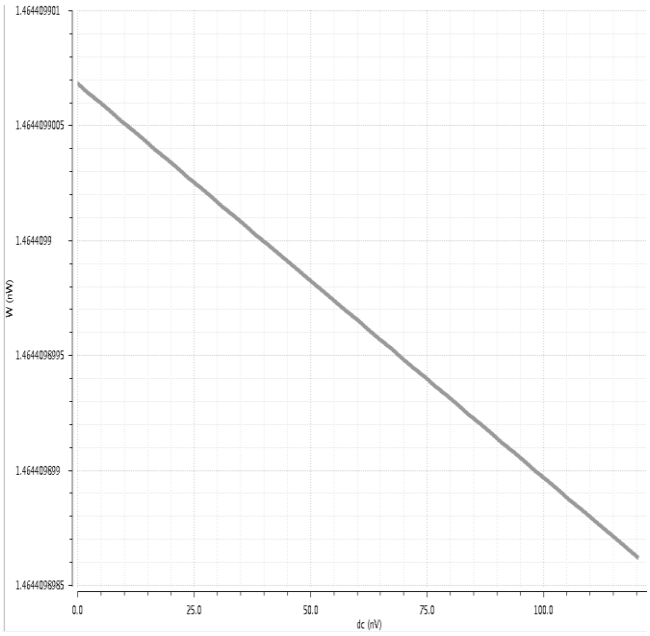


Figure 8. Static power wave form of the proposed design

The static power is calculated to be 0.029E-6 i.e., $P_{static} = 0.029E-6$ *W*. The dynamic power can be calculated by applying pulse to the inputs *a*, *b* and c_{in} and by doing transient analysis of the circuit. The output is connected with capacitor and the output waveform is calculated by selecting the capacitor connected wire. The dynamic power plot is shown in Fig. 9.

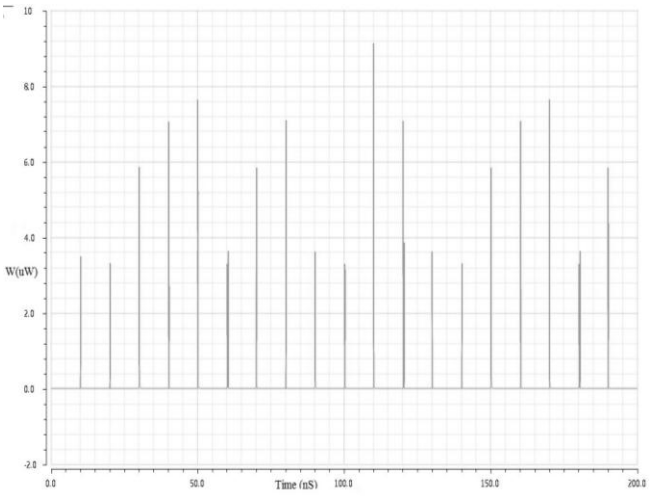


Figure 9. Dynamic power plot of the proposed design

The Dynamic power is found to be 1.981 E-6 i.e., $P_{dynamic}$ = *1.981E-6 W.*

The total power or average power is found out by adding P_{static} and $P_{dynamic}$.

Hence P_{avg} = *(0.029E-6 + 1.981E-6)W.*

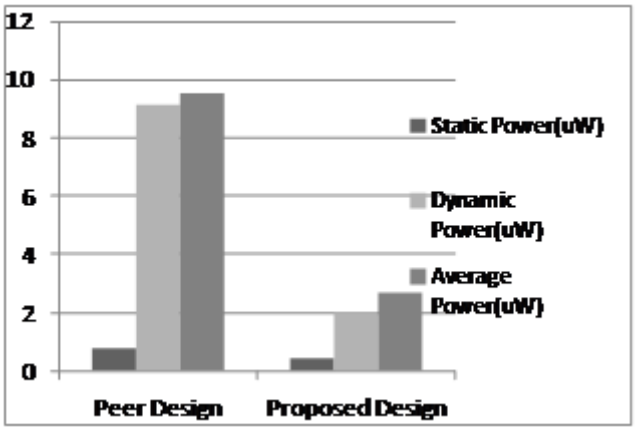
P_{avg} = *2.010E-6 W.*

This power is calculated by taking supply voltage of 0.7 V. This power is compared with the power consumed by the previous design and the comparison is given in Table 1.

TABLE 1 COMPARISON OF POWER CONSUMPTION BETWEEN PREVIOUS DESIGN AND PROPOSED DESIGN

Design	Static Power	Dynamic Power	Total Power
Previous Design	0.413E-6	9.135E-6	9.548E-6
Proposed Design	0.029E-6	1.981E-6	2.010E-6

Based on the above table data the following chart is obtained which shows the comparison of power consumption and circuit delay by the proposed full adder circuit and the previous full adder circuit.



From the above table it is clear that the modified design reduces the power consumption of about 79% and this will be an advantage in future designs.

V.CONCLUSION

In this paper we proposed a modified design of 10Tfull adder circuit using DG-MOSFET. Double gate MOSFET technology achieves low power consumption and appreciable performance of the device with elevated speed. The proposed modified design will reduce the average power nearly by 79% as compared to the previous design and the static power or the leakage power is reduced about 93% in this modified design. Simulation results of the proposed design is done with Cadence virtuoso with 45nm technology.

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